Semiconductors

Book S14 1988

Liquid Crystal Displays and Driver ICs for LCD

Liquid crystal display

Contents

Preface

PREFACE

This data handbook incorporates information about LCD cells, LCD modules and driver ICs for LCD.

LCD cells are versatile displays with a large number of superior features. These include low power consumption, high legibility (even in bright sunlight), thin outline and flexibility in pattern design, making them very suitable for customization.

Modules are the incorporation of LCD cells and IC drivers into one unit. The thin outline of the cells enable the module to remain compact and easy to mount in a variety of applications. We offer both full-dot graphic and character display modules in twisted nematic (TN) liquid crystal technology (see the chapter "User guide").

With the advent of supertwisted nematic (STN) technology, the application areas of LCD have expanded enormously. STN creates the possibility of high information density displays with far better viewing angles and contrast than TN displays (see the section Derived technologies of the chapter "User guide").

Driver ICs for LCD can be both dedicated and non-dedicated microcontrollers or microprocessors. Full data is included in this handbook for the dedicated devices and brief data is included for the non-dedicated devices.

As LCDs can be custom designed the handbook contains a custom design section and a pull out order form for completion by the prospective customer.

For more information on the principles of LCD refer to the chapter "User guide". Standard cell data is contained in the chapter "LCD data" and module data for twisted nematic modules is contained in the chapter "LCD module data". Data for driver ICs is contained in the chapter "Driver ICs for LCD".

Selection guide

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LCD cells

* DD = direct drive

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LCD modules

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LTD203

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LTD211

7Z22300

LTD101

7Z22295

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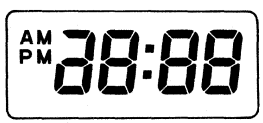

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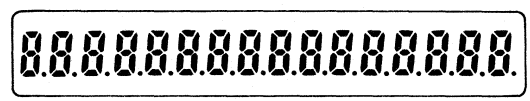

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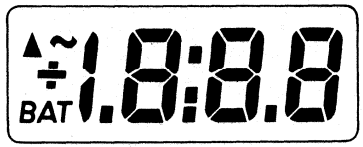

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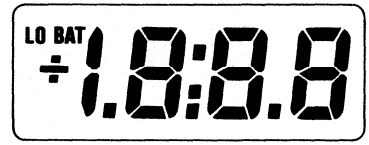

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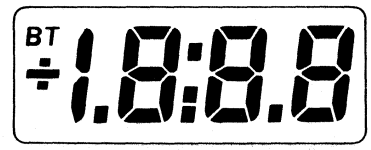

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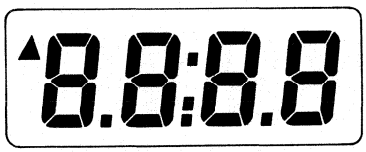

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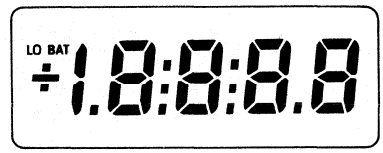

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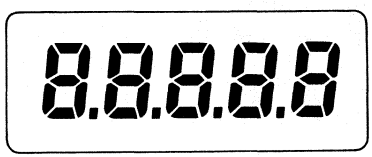

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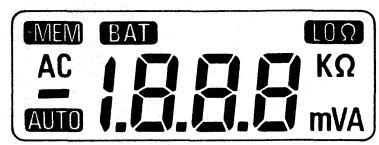

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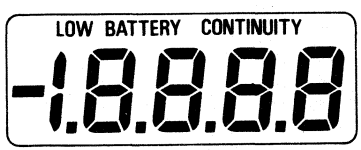

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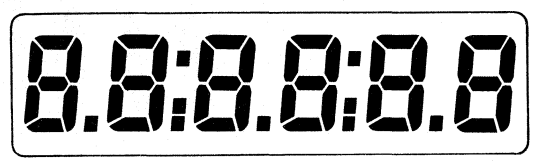

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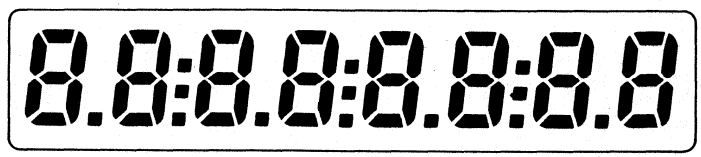

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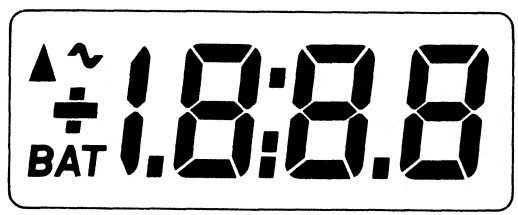

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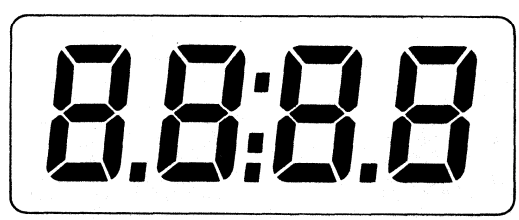

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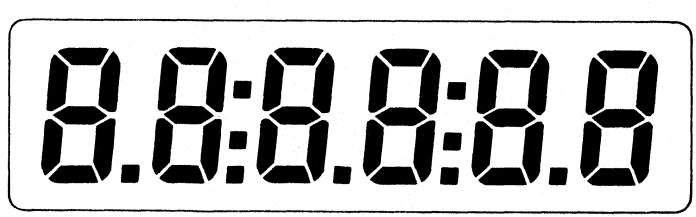

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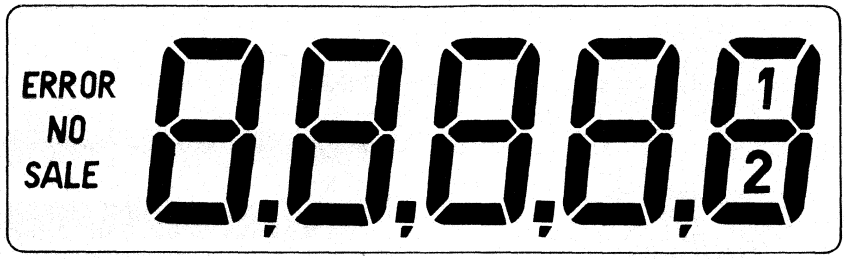

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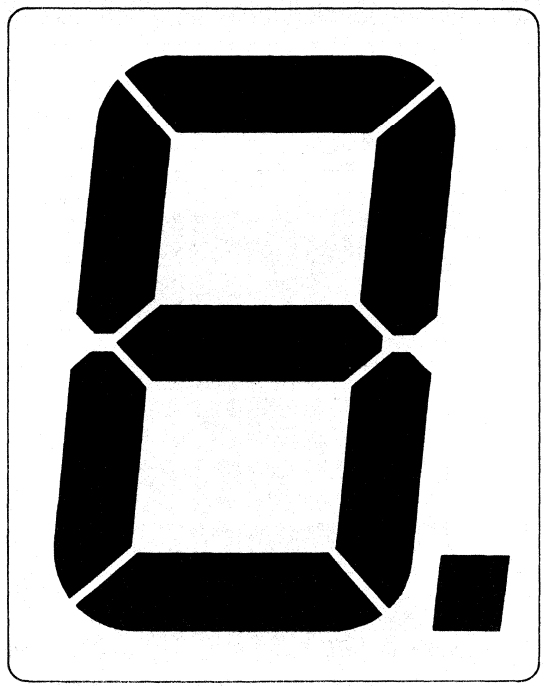

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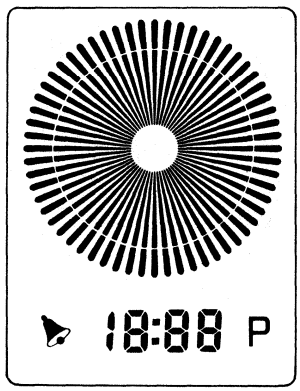

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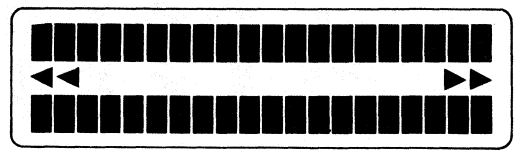

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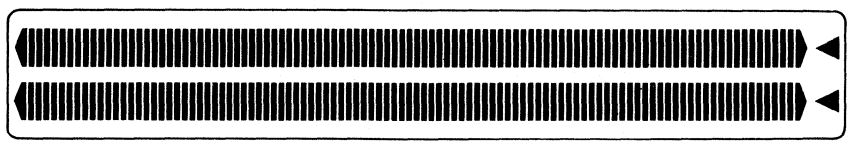

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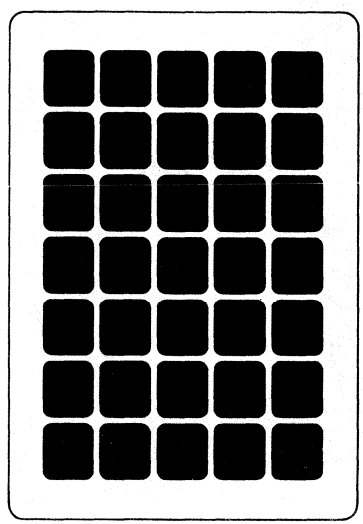

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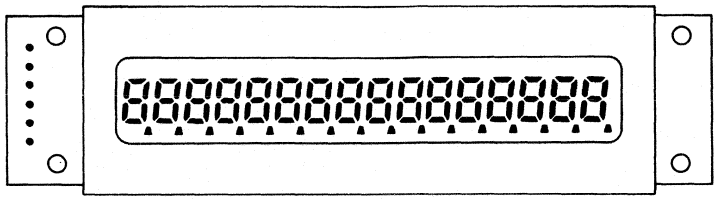

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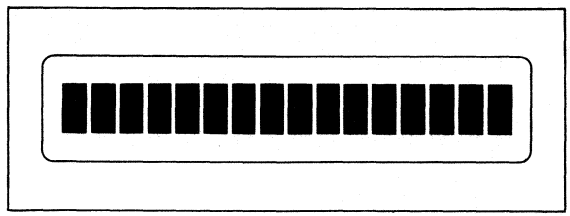

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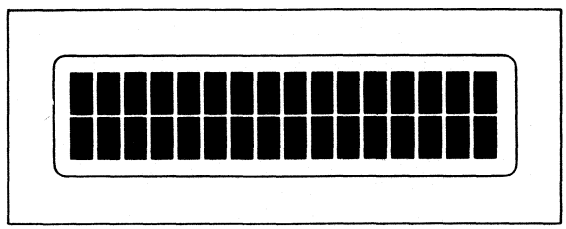

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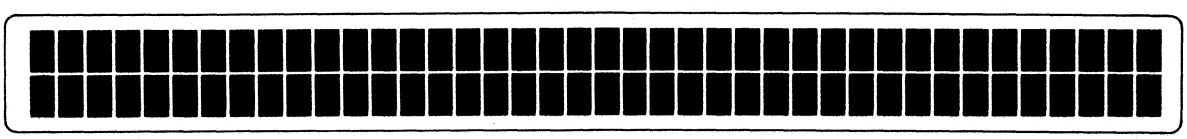

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INTRODUCTION

Liquid crystals are materials which combine the properties of both liquids and crystals. Rather than a melting point they have a temperature range, known as a mesophase, within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to that of a solid crystal.

Around 1970 it was found that thin layers of a certain type of liquid crystal can be switched from transparent to opaque or vice-versa, by application of a voltage. This property is the fundamental operating principle of all Liquid Crystal Displays (LCDs).

The main advantages and features of LCDs are:

- Flat and compact size: LCDs are lightweight and very thin; the thickness of the display is only a few millimeters
- Low power consumption: low power and supply voltage requirements mean that they can easily be powered over long periods by batteries and at the same time be compatible with modern electronic circuits e.g. CMOS
- Passive display: LCDs do not generate light and as such are comparable to printed material. One needs light to read the display and it does not fade as the ambient light increases. Reading in dark conditions is possible with the use of back lighting
- Reliable: LCDs have a wide operating temperature range and a long life
- Flexible design: a change in display size or layout is relatively simple, making LCDs very suitable for customization
- Low cost: LCDs are the most economically produced flat display system, including drive and supply aspects

Initially LCDs were used almost exclusively in watches, calculators and measuring instruments. These were simple, usually seven segment displays with a limited amount of numeric data. More recent advances in technology have extended legibility, information content and the temperature range, which has lead to applications in telecommunications, cars, entertainment electronics and computers.

LCDs are now the fastest growing display technology. They are currently replacing the CRT for the display of text and graphics and may eventually replace the CRT in TV applications.

STRUCTURE OF AN LCD

An LCD consists of two glass plates which are sealed together with a gap between them of 6 to 10 μm (Fig.1). The inner surfaces of the glass plates are coated with transparent electrodes which define the characters, symbols, or other patterns to be displayed The electrode material is usually Indium/Tin Oxide (ITO).

Between the electrodes and the liquid crystal there are polymeric layers which are treated in a way that induces the adjacent liquid crystal molecules to maintain a defined orientation angle. For this reason, the polymeric layers are also know as the orientation or alignment layers.

The distance between the two plates is set within narrow limits by means of glass fibre spacers or minut plastic balls.

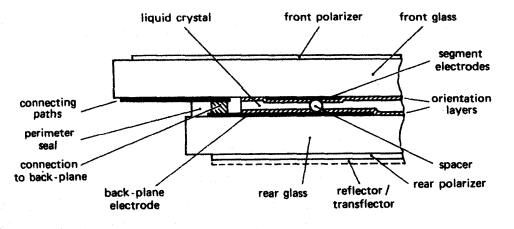


Fig.1 Construction of a liquid crystal display.

Liquid crystal

The most common type of liquid crystal used in displays is nematic (Fig.2(a)). In nematic liquid crystal the long rod-like molecules align themselves spontaneously parallel to each other which gives the material anisotropic optical and electrical properties, i.e. it has different properties in different directions. Other classes of liquid crystal which are increasing in significance for displays are cholesteric (Fig.2(b)) and smectic (Fig.2(c)).

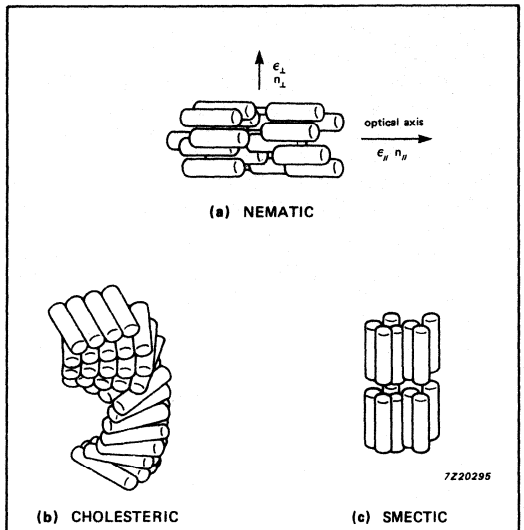


Fig.2 Molecular structure of liquid crystals (a) nematic (b) cholesteric (c) smectic.

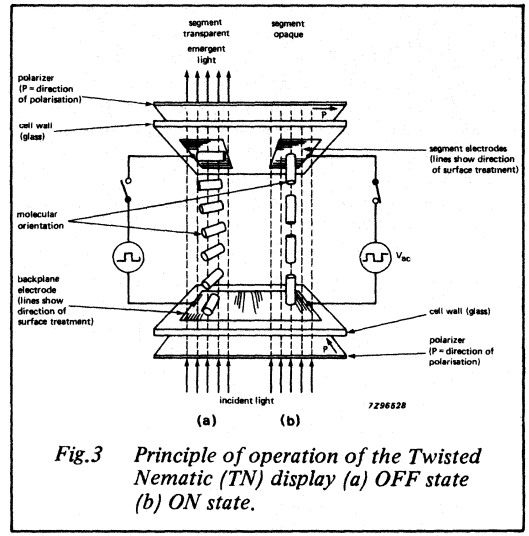


Fig.3 Principle of operation of the Twisted Nematic (TN) display (a) OFF state (b) ON state.

THE TN LCD IN OPERATION

The operating principle of Twisted Nematic (TN) LCDs is illustrated in Fig.3. The nematic liquid crystal molecules are anchored in a fixed direction at the top and bottom plates by the orientation layer. As the orientation directions of the top and bottom plates differ by an angle of 90° the crystal molecules are twisted through a 90° helix between the two plates. Polarizing filters are aligned with the orientation directions at the respective sides. Polarized light from the bottom polarizer is then guided by the crystal molecules through the helix to the top plate with its polarization direction rotated by 90°. This property is caused by the optical anisotropy of the molecules. As such the polarization direction is aligned with the top polarizer and the light passes unhindered through it to give the display a bright appearance (Fig.3(a)).

If sufficient voltage is applied across the electrodes the electrical anisotropy of the molecules will cause them to align with the electric field and the 90° twist in the optic axis will be distorted. The light will then pass through the liquid crystal but will maintain its polarization direction and will be absorbed by the second polarizer (Fig.3(b)). On switching off the initial state is restored and the cell is again transparent. Under these conditions the display will appear black when ON and bright when OFF which is known as a positive image display.

If one polarizer is rotated through 90° the effect will be reversed and the display will appear black under no voltage field conditions and bright when a voltage is applied which is known as a negative image display.

When the electrodes completely cover the top and bottom plates the LCD will act as a light shutter. A more usual arrangement is for the electrodes to be patterned such that specific segments can be switched to form numbers, letters, or graphics. An example of this is the basic seven segment digit shown in Fig.4. Any number can be displayed by switching on the appropriate electrodes that form the various segments. It should be noted that segments are only formed where the segment electrodes and the common (backplane) electrode overlap; the remaining parts of the electrodes are required for connections to the outside.

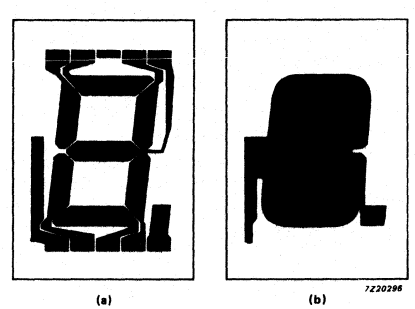


Fig.4 A seven segment plus decimal point display (a) segment electrodes (b) common electrodes

ILLUMINATION MODES

LCDs can be operated in one of three modes, depending on the ambient light conditions:

- Reflective mode: where the LCD is backed by a diffuse metallic reflector, such as brushed aluminium foil, that reflects ambient light back through the display. This mode is best suited to applications where there is always sufficient ambient light. Reflective mode is especially suited to battery operated displays as no lighting power is required (Fig.5(b)).
- Transmissive mode: where the display is lit from behind. Negative image displays are best suited to this mode. Their appearance is similar to active displays such as Light Emitting Diodes (LEDs), Vacuum Fluorescent Displays (VFDs) etc. This type of display can be projected like a slide (Fig.5(a)).
- Transflective mode: is a combination of transmissive and reflective modes. The display is backed by a partly transmissive reflector (transflector) which reflects ambient light as well as transmitting diffused back-lighting for night use (Fig.5(c)).

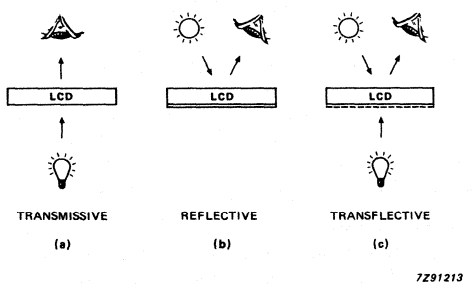


Fig.5 The three LCD illumination modes: (a) transmissive (b) reflective (c) transflective.

COLOUR IN TN LCDs

Colour can be introduced into a TN display in three ways: colour selective polarizers, coloured filters and coloured back-lighting.

Colour selective polarizers produce coloured segments on a bright background or bright segments on a coloured background. By using two colour selective polarizers a two colour combination can be produced, for example red and green polarizers will give red segments on a green background or vice versa.

Coloured filters may be either foil behind the display or translucent colours printed onto the display itself. They are best suited to transmissive mode LCDs with a negative image i.e. coloured segments on a dark background.

Coloured back-lighting produces black segments on a coloured background or coloured segments on a dark background. It is possible to change the colour of the display by using two different coloured backlights e.g. between red and green, and by using both lights, white. It should be noted that the colour effect in a transflective display will be greatly reduced under high ambient light conditions.

OPTICAL PROPERTIES

Contrast and brightness

The legibility of an LCD depends on a variety of factors such as pattern layout, technology, driving and illumination conditions, viewing direction, viewing angle, viewing distance and operating temperature. The most important optical characteristics that define legibility are brightness and contrast ratio.

The brightness of an LCD is expressed as the luminance of the reflected or transmitted light compared to the luminance of the incident light. For a reflective LCD an MgO surface is used as a reference for testing luminance. The brightness of a TN LCD cannot be higher than 50%, since an ideal polarizer only transmits half the incident light. A reflective display will, therefore, tend to appear rather grey. A brighter display can be obtained by using backlighting.

The contrast ratio (C_R) of an LCD is the ratio between the brightness of the light areas (B_l) and the brightness of the dark areas (B_d) of the display.

$$\text{i.e. } C_R = B_l/B_d$$

For a TN display the typical maximum contrast ratio can range from between 5 and 50.

In a reflective display, the maximum contrast ratio that can be detected by the human eye is normally about 10 and the lower limit of good legibility, about 2. For comparison the contrast ratio of this page is about 7.

A higher contrast ratio is necessary for back illuminated displays; especially for negative image displays, as the human eye can easily detect light leaking through the dark background of a display. The leakage can be reduced by matching the spectral transmission of the background and spectral emission of the backlighting system correctly (especially if a colour filter is used).

Both brightness and contrast depend on the type of polarizers used. For reflective displays with a positive image, low efficiency polarizers produce brighter displays with a low contrast. High efficiency polarizers produce a high contrast but will reduce brightness considerably.

Viewing angle

A twisted nematic LCD has a preferred viewing direction (φ_{pref} measured in the plane of the LCD), which is built-in during the manufacturing process by treatment of the orientation layers. For most standard applications this preferred direction is from below (6 o'clock direction) although other directions can also be manufactured.

Fig.6 shows a contrast versus voltage curve from three different viewing angles α which are referenced perpendicularly to the LCD. At a very low voltage the display is not visible; as the voltage is increased the pattern first appears at low elevation angles (high values of α) in the preferred viewing direction (curve 2). By further increasing the voltage the pattern becomes more visible at higher elevation angles. If the contrast is observed at a fixed drive voltage within the plane φ_{pref} and perpendicularly to the LCD the viewing angle is α_{opt} and maximum contrast occurs. At higher voltages the value of α_{opt} becomes rather small. However, $\alpha_{opt} = 0$ can never be reached and a basic asymmetry will always remain.

The voltage at which a display becomes visible (10% of maximum contrast) at a specific viewing direction and viewing angle, is known as the threshold voltage (V_{th}). The voltage at which contrast reaches 90% of its maximum value is known as the saturation voltage (V_{sat}).

Voltage and contrast characteristics will vary for different liquid crystal mixtures. Most mixtures will also have a negative temperature coefficient i.e. V_{th} decreases as the temperature increases.

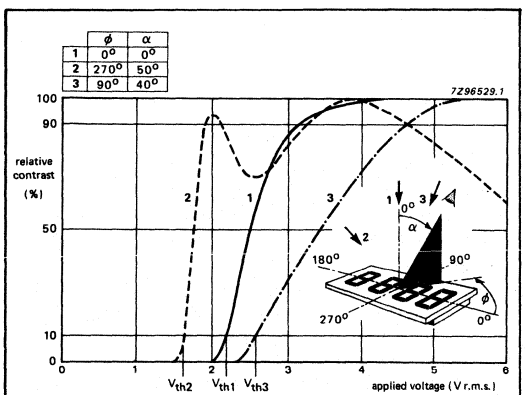


Fig.6 Relative contrast as a function of applied voltage.

When in a plane perpendicular to φ_{pref}, TN LCDs have an almost symmetrical contrast. This is shown by an isocontrast diagram which is a method of illustrating the viewing cone of a display. An isocontrast diagram is the contrast in relation to the azimuth (φ) and elevation (α) viewing angles. Figure 7 is a typical isocontrast diagram for a TN display which has a preferred viewing direction from below (6 o'clock).

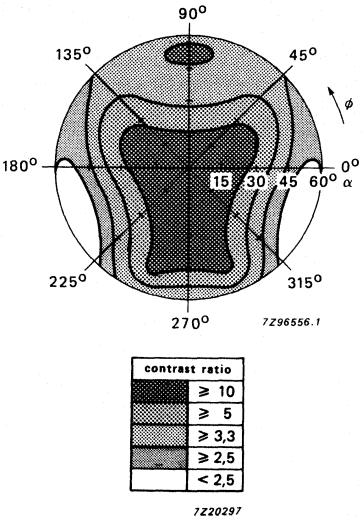


Fig.7 Typical isocontrast diagram for a direct-driven, reflective TN display, showing the variation of contrast as a function of the two components α and ϕ of the viewing angle.

Response times

Typical turn-on and turn-off times for LCDs range between 50 and 100 ms at room temperature. One of the main influences upon response times is the liquid crystal viscosity. As the viscosity of the material increases with decreasing temperature the molecules become less free to move resulting in longer response times.

Response times are also affected by applied voltage, drive method and liquid crystal layer thickness.

DRIVING LCDs

Each segment of an LCD can be considered the equivalent of an electrical capacitance with a very high parallel and low series resistance (Fig.8). The capacitance is voltage dependent as the liquid crystal molecules have anisotropic dielectric properties. Applying a DC voltage will cause electro-chemical reactions which shorten the life of the LCD. For this reason, the drive voltage must be alternating with a maximum permissable DC component of 100 mW. The optical effect then produced in a display depends approximately on the rms value of the drive voltage.

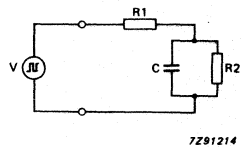


Fig.8 Simplified equivalent circuit of an LCD. R_1 is the series resistance of the electrodes. R_2 the series resistance of the liquid crystal and C the interelectrode capacitance.

Typical values are $R_1 = 10\ k\Omega$, $R_2 = 1\ M\Omega/cm^2$, $C = 1.5\ nF/cm^2$.

The frequency of the drive voltage must be at least 30 Hz to prevent display flicker. At this frequency and a drive voltage just above the saturation voltage, typical current consumption is approximately 1.5 μA per square centimetre of the activated display area.

The current consumption increases in direct proportion to the drive frequency. An upper frequency limit is set by coupling and relaxation effects which cause ghosting and irregular contrast in the display. These effects must be considered, especially in the layout of large and complex displays. The upper frequency limit is approximately 200 Hz.

Possible interference effects with lighting systems should also be considered when deciding on the drive frequency to be used.

Direct Drive

A direct (or static) drive LCD has a separate connection and driver for each segment and one for the common back-plane.

The back-plane of a direct drive display is usually driven by a square wave having a peak-to-peak value (V_{op}) that is above the saturation voltage (V_{sat}). To select a segment, the inverse of the back-plane waveform is applied to the appropriate electrode. This produces an rms voltage between the back-plane and segment electrodes which is equal to V_{op}. The back-plane voltage waveform is also applied to all non-selected segments which results in a net zero voltage across them. It should be noted that a symmetrical square wave must be used, otherwise undesirable DC components will be applied to the liquid crystal.

Fig.9 illustrates a typical direct drive circuit with exclusive-OR gates controlling the voltage to the different segments. Individual segments are selected by switching the appropriate segment control line HIGH. This will have the effect of inverting the back-plane voltage applied to the segment. The control lines of non-selected segments are LOW so that no inversion takes place.

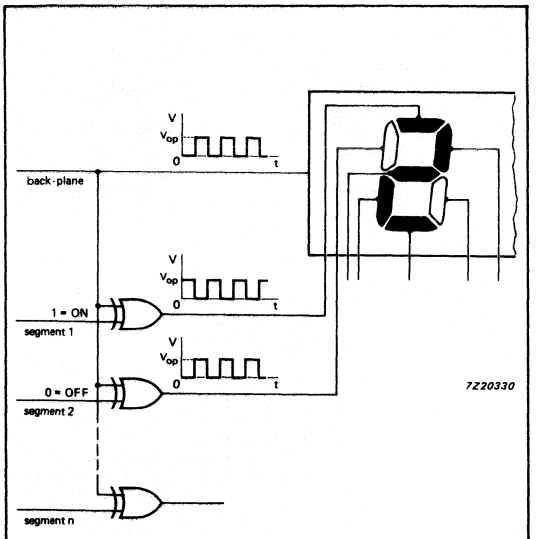


Fig.9 Phase-switching circuit for direct-drive.

The advantage of direct drive are broad temperature ranges, wide viewing angles, fast response times and insensitivity to driving voltage tolerance. However, the number of connections and driving circuits needed can become very large for complex displays.

Multiplex Drive

In high information density displays, such as a dot matrix, it is difficult or impossible to connect each dot or segment individually to an edge contact. The large number of contacts and drivers required could lead to low reliability and high cost. Therefore, it is necessary to use multiplex drive.

Multiplex drive electrodes are arranged in the form of a matrix. Segments are connected in groups and the back-plane is split into several commons so that every segment in a group has a different back-plane. A segment is then no longer identified by an individual external contact but by a group contact and a specific back-plane. The multiplex ratio is defined as 1:N, where N is the number of back-planes, or segments, per group.

Fig.10 illustrates the segment to back-plane assignment for a seven segment digit using 1:3 multiplex drive. The number of contacts needed has been reduced from the nine used in direct-drive, to six. Fig.10(c) shows the equivalent circuit with each segment being represented by a capacitor.

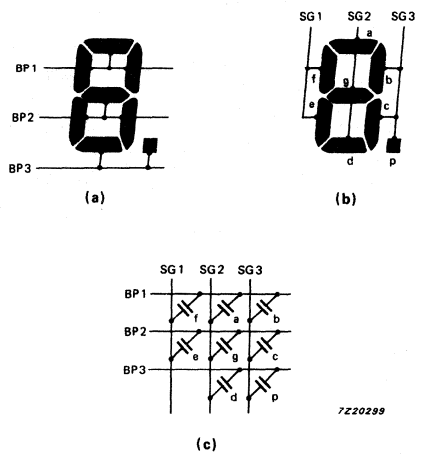


Fig.10 A single digit plus point, 8 segment LCD with 1:3 multiplex drive (a) Back-plane electrodes (b) Segment grouping (c) Equivalent circuit.

The reduction in the number of contacts required by using multiplexing can be dramatic. A segment display having a multiplex ratio of 1:N and a total of M segments can be addressed using as few as M/N + N connections.

For example:

- a 40 segment display requires 41 connections in direct drive but, by using a 1:4 multiplex drive, the number of connections is reduced to:

  $$40/4 + 4 = 14$$

- a dot matrix display with 20 000 elements (pixels) i.e. 100 rows and 200 columns can be controlled with only 300 connections (number of rows + number of columns) rather than the 20 001 connections that would be needed for direct drive.

An individual segment is selected by a combination of the back-plane and segment group signals. Fig.11 shows a simple example of matrix waveforms. Each back-plane is selected in sequence and whether or not a segment is selected is determined by the level of the segment group voltage when the corresponding back-plane is addressed. The waveforms illustrated have net DC components which could cause electromechanical degradation of the liquid crystal. In practical addressing schemes, the net DC component is eliminated by inverting both the back-plane and segment group waveforms alternately.

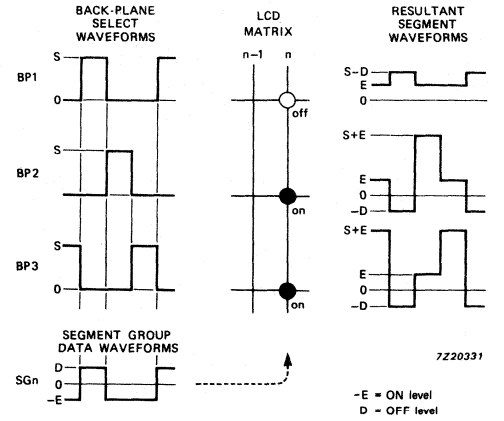


Fig.11 Row and column multiplexing waveforms for a display showing the voltage waveforms across individual elements.

Fig.11 shows that all of the elements receive a voltage. This means that the voltage at which non-selected elements should remain OFF has been raised above zero. The ratio of the ON to the OFF voltage (discrimination) decreases as the multiplex ratio increases (see Table 1) and the non-selected elements will become slightly visible. The discrimination can be optimised up to a certain limit, by increasing the number of multiplex levels.

Table 1 shows that the largest relative profit is obtained when going from direct drive to MUX 1:2 drive The number of connections is approximately halved but a reasonably good discrimination is obtained (2.24). Which is why MUX 1:2 is popular for displays up to 100 . . . 150 segments (higher MUX rates would give little or no advantage, while reducing the contrast relatively fast).

Table 1 Discrimination and number of connections compared to the multiplex rate

multiplex ratio	1:1	1:2	1:3	1:4	1:8
discrimination, $\frac{V_{on(rms)}}{V_{off(rms)}}$	∞	2.24	1.92	1.73	1.45
number of connections required for a display having 120 segments	121	62	43	34	23

ELECTRO-OPTICAL CHARACTERISTICS OF MULTIPLEXED LCDs

Most applications require the OFF elements to remain invisible up to a certain viewing angle (α). Which means, in order to keep the OFF voltage below the threshold (V_{th}) the value of the operating voltage (V_{op}) must not exceed a maximum criteria (Fig.6). However, for ON elements a minimum contrast at a different viewing angle is required, which calls for a value of V_{op} that exceeds a minimum criteria.

Since V_{th} is temperature dependent, both ON and OFF criteria of V_{op} vary with temperature (see Fig.12 for MUX rates 1:2 and 1:8). The area between the ON and OFF criteria is the recommended operating area because it represents invisible OFF segments and ON segments with sufficient contrast.

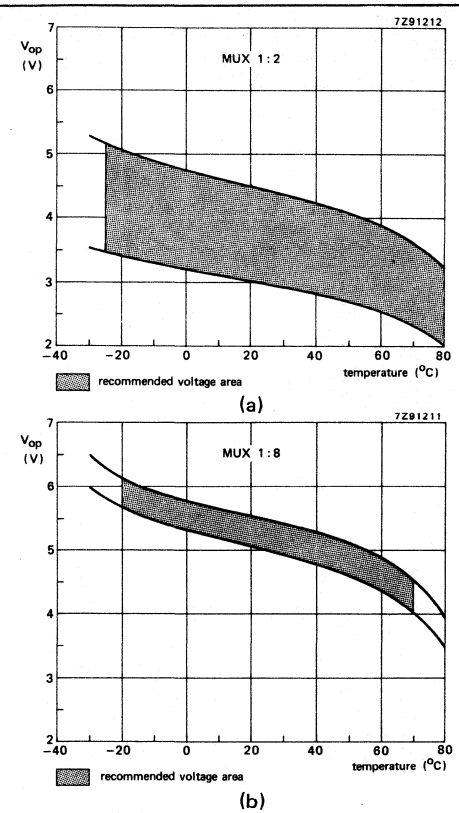


Fig.12 Typical recommended voltage areas for (a) 1:2 (b) 1:8 multiplex drive. At the lower boundary of each area the off segments become faintly visible at a viewing angle $\alpha = 40°$, $\phi = 270°$ while the ON elements are visible with a contrast better than 2 at $\alpha = 0°$.

At low multiplex ratios satisfactory operation over a wide temperature range can be obtained with a fixed value of V_{op}. However, in order to obtain a constant viewing cone throughout the same temperature range at higher multiplex ratios, V_{op} has to be temperature compensated to allow for the negative temperature coefficient of V_{th}.

Besides its effect on the operating voltage and temperature range, increased multiplexing also narrows the viewing cone (Fig.13).

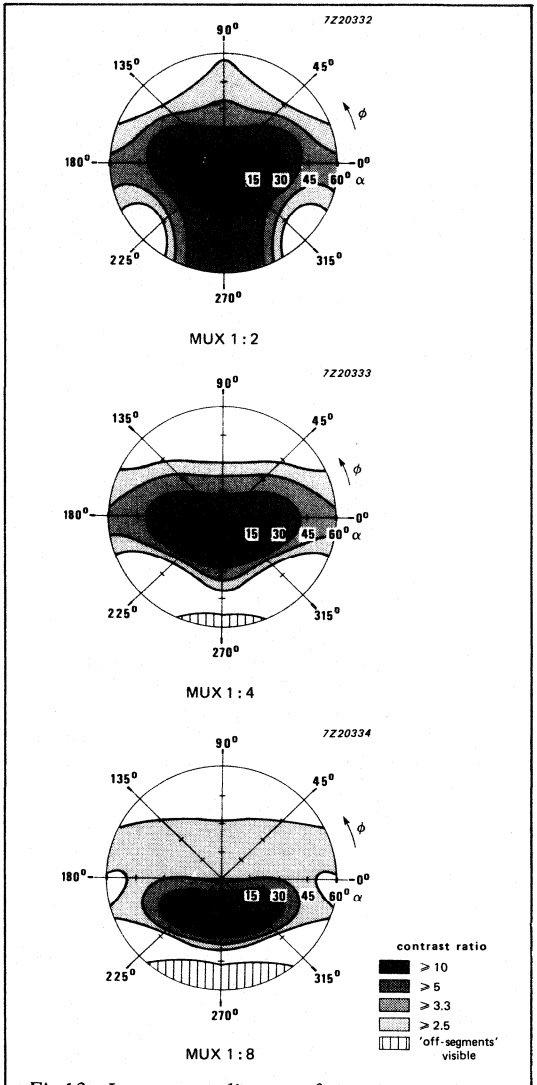


Fig.13 Isocontrast diagrams for various multiplex ratios.

The effect of OFF segments being visible depends upon the type of display pattern. In a segment display incorrect information may be displayed and the multiplex ratios are therefore, normally limited to 1:8. In character or full dot matrix displays visible OFF segments can result in somewhat darker background which is disturbing but the information is still correct and readable up to a multiplex ratio of about 1:100. Satisfactory operation at higher multiplex ratios is obtained using advanced technologies like STN displays.

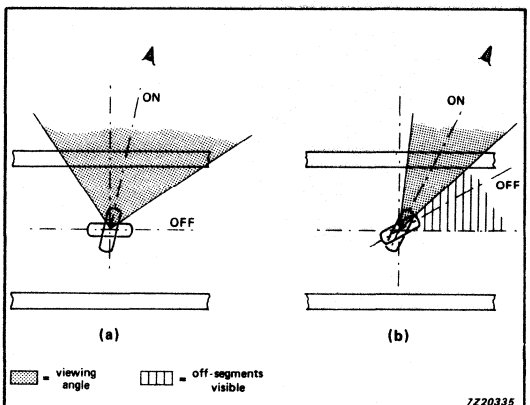


Fig.14 Angular variations of the centre liquid crystal molecule (a) direct drive (b) full multiplex drive.

DERIVED TECHNOLOGIES

Super Twisted Nematic (STN) displays

The main limiting factor in the use of a multiplexed TN display is the gradual slope of the contrast as a function of the voltage curve. It has been discovered that this curve can be made much steeper by increasing the twist angle of the crystal beyond 90° to a value that ranges from 180° to 270°.

The larger twist angle is achieved by using a special cholesteric doped nematic liquid crystal. The cholesteric molecules have a helical screw structure (Fig.2) which helps to ensure that all liquid crystal molecules twist in the same direction and have the same stable state.

STN displays use birefringence effect which introduces wavelength dependence and a characteristic colour into the display. With optimized polarizer angles the display will e.g. appear blue on a bright background (blue mode) or bright on a yellow background (yellow mode).

STN displays can produce images with a good contrast over wide viewing angles at multiplex rates of 1:100 or higher.

Guest-Host Display (GHD)

Two problems associated with TN displays are the angular dependence of the contrast and the relatively low brightness. These are both caused by the use of two polarizers. An alternative type of display is the Guest-Host Display (GHD) which works with one or no polarizers. In GHDs the molecules of a dichroic dye (guest) are dissolved into the nematic liquid crystal (host). The guest molecules always align themselves parallel to the molecules of the liquid crystal.

When there is no voltage applied the molecules are aligned parallel to the display surface (OFF state) certain wavelengths of the incident light are absorbed by the dye and the display appears coloured. When sufficient voltage is applied the molecules will align perpendicular to the display (ON state), the dye no longer absorbs the light and the display appears bright (Fig.15). GHDs typically have bright segments on a coloured background, the colour of which depends on the dye and can include black.

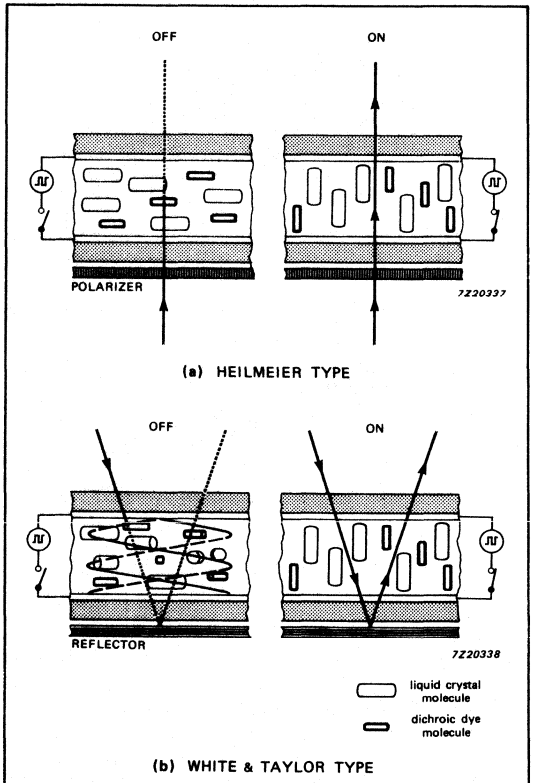


Fig.15 Operation of a GHD (a) Heilmeier (b) White and Taylor.

There are two main types of GHD:

- Heilmeier (Fig.15a). This display requires a front polarizer for good legibility and must have good backlighting or be viewed in good ambient light conditions.
- White and Taylor (Fig.15b). This display is optimized for reflective operation because it does not require polarizers and produces very bright segments against a coloured or grey background.

The advantage of guest-host displays over twisted nematic displays is the very wide and regular viewing cone. Disadvantages are the higher operating voltage and poor multiplexibility.

CONNECTING TECHNIQUES

The terminals of an LCD are Indium/Tin Oxide and are situated on at least one side of the cell.
The three main methods used to electrically connect LCDs are: fixed pins, conductive rubber (elastomer) strips and foil.

Fixed pins are glued directly onto the LCD which can then be soldered directly on to a PC-board or connected via snap-on sockets (Fig.16(a)). Fixed pins are suitable for LCDs with a relatively low number of connections and the glass length is sufficient to accommodate the required pins. However, they provide a reliable method of contact.

Elastomer connectors consist of alternate conductive and insulating sections that support the LCD and connect it to the PC-board (Fig.16(b)). The contacts of the LCD are on the underside of the top glass and these connect to the PC-board via the conducting sections of the elastomer strip. Contact is maintained by a mounting bezel or clamp which squeezes the LCD, elastomer strip and the PC-board together. Care must be taken to ensure that a constant pressure is maintained over all the connections which requires special attention in long displays. Without optical alignment a contact pitch down to about 1 mm can be used and down to about 0.5 mm with optical alignment.

Foil connectors (Fig.16(c)) provide a flexible method of connection for LCDs. They consist of parallel conductors mounted on a foil which is glued directly on to the LCD; the contact area is thus sealed from the atmosphere. Connection pitches at each end of the foil can vary and the drivers can be mounted on a remote printed circuit-board which is an advantage where a very thin display or back-lighting is required.

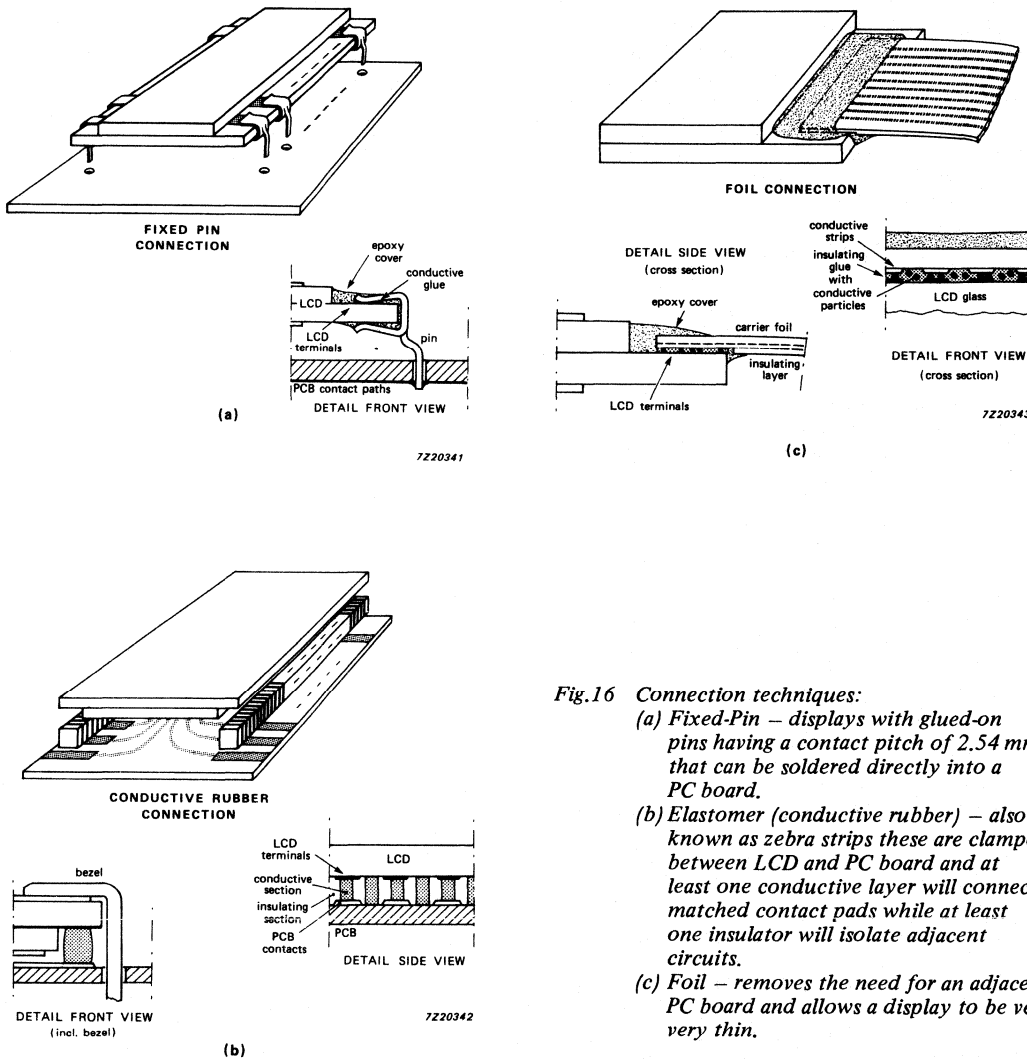


Fig.16 Connection techniques:
(a) Fixed-Pin – displays with glued-on pins having a contact pitch of 2.54 mm that can be soldered directly into a PC board.
(b) Elastomer (conductive rubber) – also known as zebra strips these are clamped between LCD and PC board and at least one conductive layer will connect matched contact pads while at least one insulator will isolate adjacent circuits.
(c) Foil – removes the need for an adjacent PC board and allows a display to be very very thin.

MOUNTING & ILLUMINATION TECHNIQUES

Reflective and transflective displays should be mounted as close as possible to the front surface of the equipment to gain maximum illumination from the ambient light. When choosing a mounting position the viewing angle and isocontrast diagram published in the LCD data sheet must be considered. Auxiliary front lighting for a reflective display should be at an angle close to the normal viewing direction to minimise reflection and shadow effects.

Mounting pressure applied to LCDs using elastomer connectors should be as even as possible and pressure on the seal or viewing areas must be avoided. Glass or non-birefringent plastic should be used to protect the frontpolarizers from scratches and humidity.

Back-lighting

Back-lighting of a transflective display is necessary to maintain legibility under poor environmental light conditions.

The main methods used for LCD back-lighting are listed below:

- Electro-luminent light-source; has the advantage that it is very thin and emits a diffuse and evenly distributed light. However, its luminance is low, it requires a supply of 100 to 200 V at a few hundred Hz and it has a limited life (Fig.17(a)).
- Light guide; a point source such as an LED or a linear source such as a fluorescent tube is distributed by a light guide using total reflection. Its construction can be flat so little space is required behind the LCD. However, uniform light distribution can be difficult to obtain and light loss can be considerable (Fig.17(b)).
- Light box; an LED, halogen or fluorescent light is distributed by a light box; this light source is very effective but needs considerable space immediately behind the display (Fig.17(c)).

Any form of back-lighting for LCDs requires considerably more power than is used by an unlit display. This is a limiting factor when using a battery power supply.

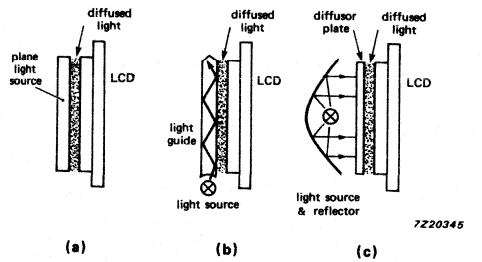


Fig.17 Back-lighting methods.

LCD modules

page

LCD modules

INTRODUCTION TO LCD MODULES

An LCD module is a liquid crystal display complete with driving circuitry, and in many applications also decoding and control circuitry which assists interfacing.

Typical applications for LCD modules include industrial display equipment, pocket VDUs, portable computers, telephony equipment, typewriters and point of sales equipment.

The internal inter-connection between driving circuitry and display can be elastomer (zebra-stripes) or flex-foil. One of the advantages of an LCD module over a loose display is that less external connections are required, allowing a mounting location which is remote from the control circuit.

The use of a complete LCD module in display equipment means a great deal less time in designing the display into the equipment, as all the driving circuitry is internal and interface to a microprocessor is the design engineers only concern.

All of our modules are light and compact and can be easily mounted into display equipment. They have a good contrast over wide viewing angles.

We offer our modules in three display modes which are:

(i) segment display modules
(ii) character display modules
(iii) dot matrix display modules

For each mode we have standard types available which are listed in **Table 2.**

SEGMENT DISPLAY MODULES

Features

- Serial interface e.g. C-bus and I²C-bus
- Low MUX rate hence good contrast and viewing angle, especially in high ambient light conditions
- Low drive voltage
- Light, compact and easy to mount

Description

Segment display modules are intended for numeric applications (though the design can include some fixed symbols). In comparison to character types the restriction in data representation allows low multiplex rates (up to MUX 1:4), good contrast over wide viewing angles and low driving voltage. A typical application for segment display modules is in telephone sets for displaying the dialled number.

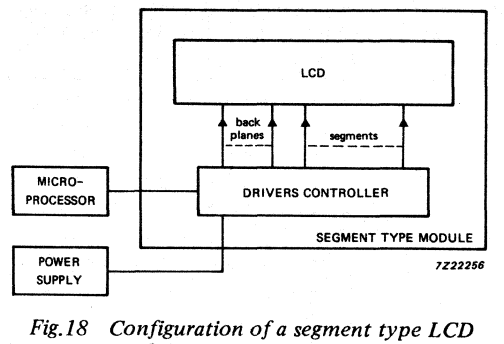


Fig.18 Configuration of a segment type LCD module.

Table 2 TN LCD module types

DESCRIPTION	ILLUM. MODE	CLASS	TYPE NUMBER
1-line, 16-digit	reflective	segment	LTM233R-10
1-line, 16-character	reflective	character	LTN111R-10
	transflective		LTN111F-10
2-line, 16-character	reflective	character	LTN211R-10
	transflective		LTN211F
2-line, 40-character	reflective	character	LTN241R-10
240 X 64 dot, full graphic	reflective	dot matrix	LTG201R-10
640 X 200 dot, full graphic	transflective	dot matrix	LTG401F-10

CHARACTER DISPLAY MODULES

Features

- Interface with either 4-bit or 8-bit parallel data input (ASCII)
- Built in controller that includes a character generator, and LCD driver functions
- Good legibility in bright light
- Light and compact and easy to mount

Description

Character liquid crystal display modules (also known as alpha-numeric displays) are light and compact modules with a controller including a character generator, LCD driver LSI-ICs and a character type LCD cell mounted on a single printed circuit board.
The built in character generator makes the design engineers task easier when incorporating one of our character modules within his equipment. It is capable of generating 168-alphanumeric, Japanese characters and symbols (160 fixed characters and 8 user programmable characters).

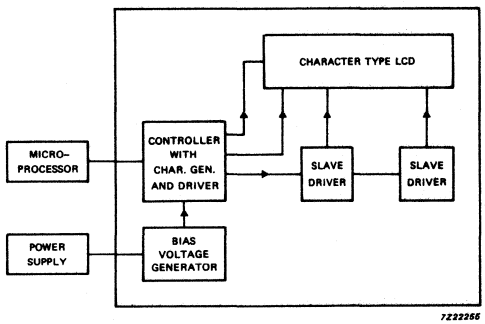


Fig.19 Configuration of a character type LCD module.

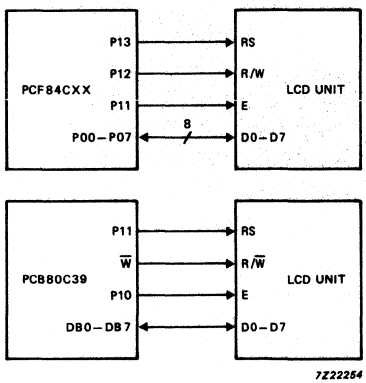
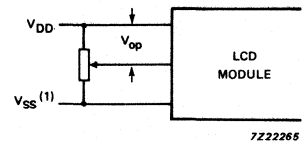


Fig.20 Microprocessor interface.



(1) for LTN241R-10, V_{SS} is to be replaced by V_{EE}, when $V_{EE} < V_{SS}$.

Fig.21 Power supply.

Our character display modules are offered with 1, 2 or 4-lines of characters and a character font of 5 X 8 (5 X 7 dots + cursor). They can be interfaced with a 4- or 8-bit parallel microprocessor and have a 1:16 multiplex drive ratio (refer to technical publication 238 for further details on character display modules).

i) Interface signals

RS	register select
R/W	read/write select
E	enable read/write
D0 to D7	input output data

ii) Supply voltages

V_{DD}	positive supply voltage for logic
V_{SS}	negative supply voltage for logic (logic ground)
V_O	contrast adjustment voltage: operational LCD voltage, V_{op} equals $V_{op} = V_{DD} - V_O$

DOT MATRIX DISPLAY MODULES

Features

- Full dot graphic display capability
- Good legibility in bright light
- Light and compact and easy to mount

Description

Dot matrix LCD modules (also known as flat panels) are capable of displaying a wide variety of data as each individual dot can be controlled ON or OFF. The dot matrix LCD module is ideal for displaying diagrams, graphs, and text.

The number of horizontal (rows) and vertical (column) electrodes multiplied gives the number of pixels or dots as a pixel or dot is located at the cross point of the electrodes. The multiplex rate is determined by the number of electrodes on the short side of the display which also determines the display technology.

To enable higher contrast when using a high MUX rate display the dot areas are separated into two display parts (upper and lower). This necessitates doubling the data bits.

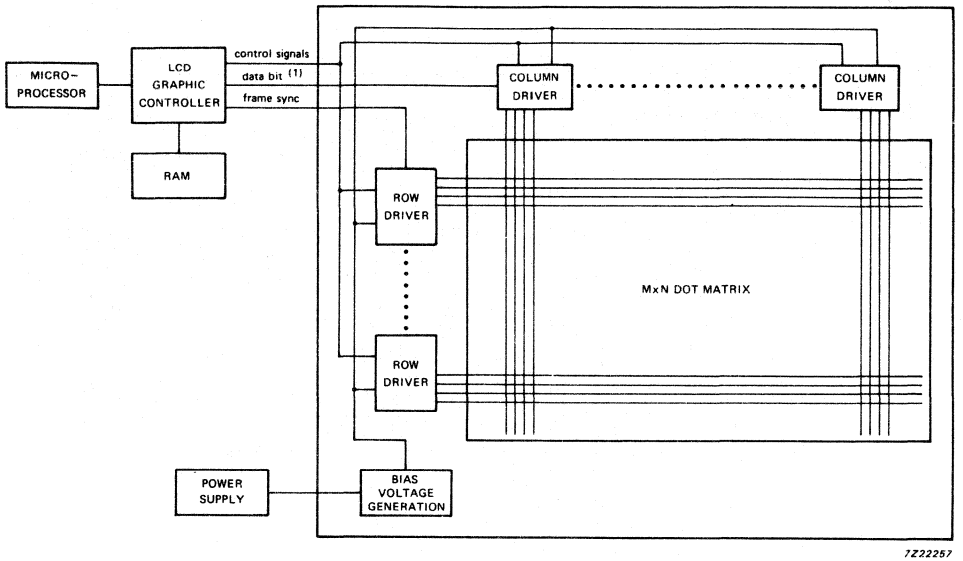


Fig.22 Configuration of graphic display module when the MUX rate is equal to the number of rows. (1) (1 bit serial or 4 bit parallel).

i) Control signals

CP1 = clock pulse 1 (latch)
CP2 = clock pulse 2 (shift)
FS = frame synchronisation
M = signal to convert the LCD drive waveform into AC

ii) Supply voltages

V_{DD}	positive supply voltage for logic
V_{SS}	negative supply voltage for logic (logic ground)
V_O	contrast adjustment voltage; operational LCD voltage; V_{op} equals $V_{op} = V_{DD}-V_O$

iii) Data inputs

a) Module with a MUX rate equal to the number of rows (Fig.22)	1-bit serial: used for displays with a relatively small number of dots 4-bit parallel: used for displays with a larger number of dots
b) Module with a MUX rate equal to half the number of rows (Fig.23)	2 X 1-bit serial: used for displays with a relatively small number of dots 2 X 4-bit parallel: used for displays with a larger number of dots

Description of input data and control signals

Currently we offer our dot matrix displays with 1-bit serial data input or 2 X 4-bit parallel data input.

On the falling edge of CP2 the input data is sequentially transferred into the shift register in the column drivers. On the falling edge of CP1 the data is latched and displayed.

The scan sequence is started by clocking signal FS in on the HIGH to LOW transition of clock pulse CP1 after which the first row is scanning and the second row information is clocked in by CP2.
When all the data of row 2 has been entered and latched on the falling edge of CP1, the display proceeds to scanning the second row.
The data input continues until the whole area of the display is filled and then proceeds to the next display face.

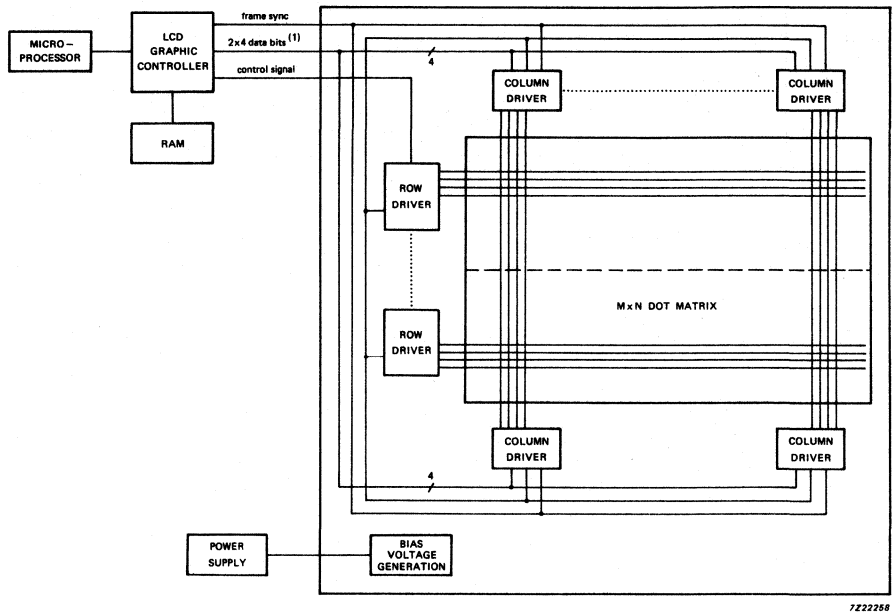


Fig.23 Configuration of a graphic display module when the MUX rate is half the number of rows. (1) (2 X 1 bit serial or 2 X 4 bit parallel).

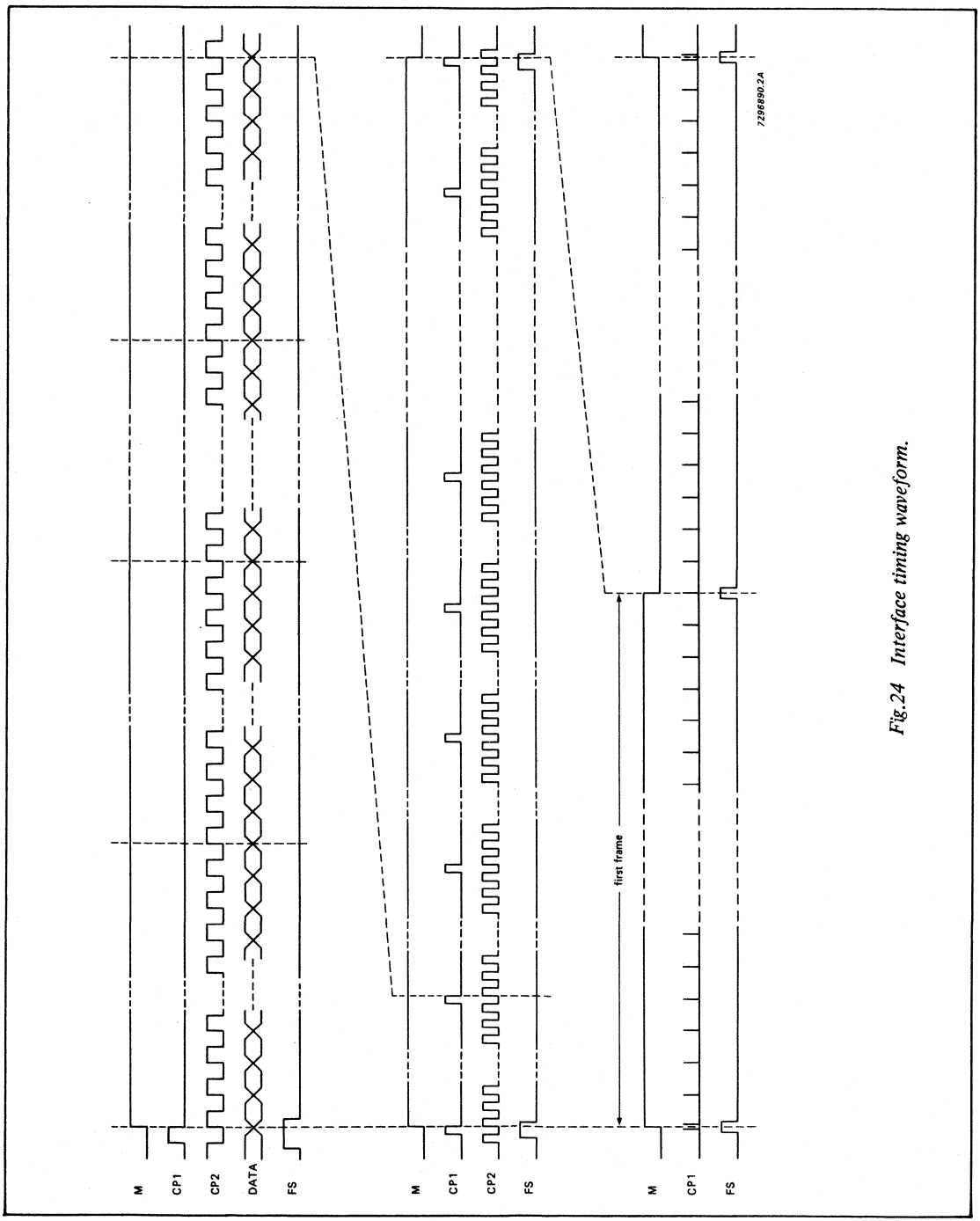


Fig.24 Interface timing waveform.

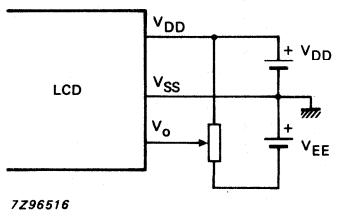


Fig.25 Power supply.

Quality

QUALITY ASPECTS

QUALITY IN DESIGN AND PRODUCTION

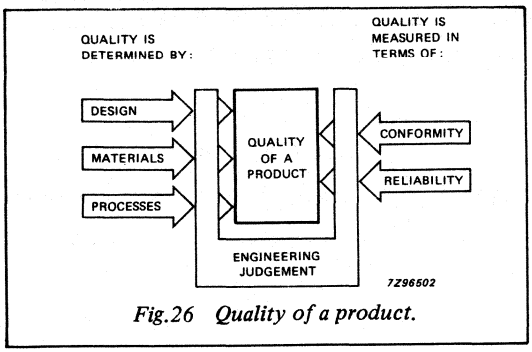


Fig.26 Quality of a product.

All appropriate aspects of quality are an integral part of our design rules for new LCD types, ensuring that quality is designed into our products from the beginning. The development of each new type of LCD is finalized by a product release procedure which inspects the quality of the design.

Our production quality assurance program is based upon internationally accepted standards. The results of tests carried out during incoming inspection, at the in-line inspection and final acceptance stages are used as feedback in order to continually improve our process and design rules.

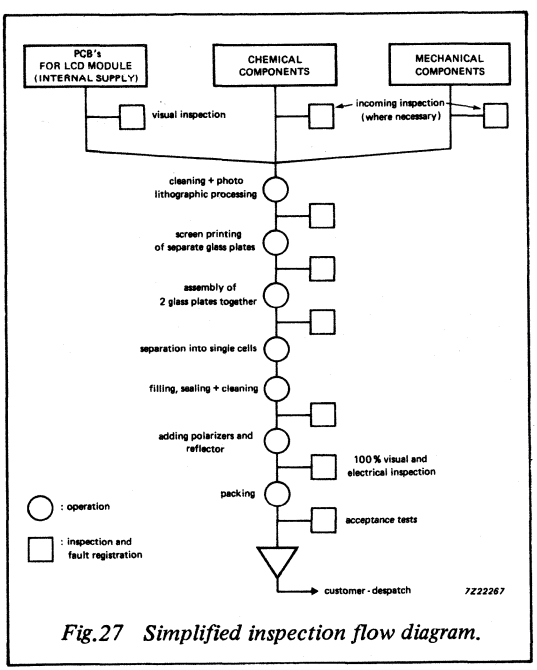


Fig.27 Simplified inspection flow diagram.

PRODUCT RELEASE

To ensure that every LCD type fulfills its specified requirements, a product release procedure is carried out at the end of the development of each new type.

This procedure guarantees that each product withstands an extensive program of environmental tests according to IEC standards and a number of suplementary tests which are specific to LCDs.

The polarizers attached to the outside of LCDs are available in distinct quality classes so we have also classified our LCDs into:

- commercial quality grade
- extended quality grade

Consequently there are differences in the product release tests (see Table 3). The remainder of the tests are listed in Table 4.

ACCEPTANCE TESTS

To ensure that the devices meet the electro-optical and mechanical specifications a statistical sampling is carried out prior to delivery, as described in ISO 9001. The following AQL values apply:

- for major defects: AQL 0.25
- for minor defects: AQL 0.65
- combined: AQL 1.0

The statistical sampling is also used to gather reliability data.

DEFINITION OF DEFECTS

Optical defects

Optical defects are defined as visible irregularities within the viewing area of a non-energized display. The limit of the acceptable size of an optical defect depends on the viewing distance and on the contrast of the optical fault.

The acceptance criteria for optical defects are defined by means of marginal samples, that represent esthetic borderline conditions of LCDs when mounted in the finished product.

Marginal samples for specific products can be agreed upon by the customer and us.

Electro-optical defects

Electro-optical defects are defined as visible irregularities within the viewing area of an energized display. All segments must be visible perpendicular to the display at the specified minimum operating voltage. In multiplex drive non-selected segments must not be visible from the viewing angle specified for OFF conditions.

Mechanical defects

Mechanical defects are defined as mechanical irregularities which do not influence the electrical or optical properties but can cause mounting problems for the customer, when they do not meet the mechanical specification.

Table 3 Product release tests, marking the difference between commercial and extended quality grades

TEST NAME	TEST DESCRIPTION	
	COMMERCIAL GRADE	EXTENDED GRADE
High temperature storage (IEC 68-2-2)	+70°C/21 d	+90°C/21 d
Low temperature storage (IEC 68-2-1)	−25°C/21 d	−40°C/21 d
Damp heat, steady state (IEC 68-2-3)	+40°C/95% RH/21 d	+80°C/90% RH/21 d
Change of temperature (IEC 68-2-14)	−25°C/30*, −>+70°C/30*, (X 10)	−40°C/30*, −>+85°C/30*, (X 10)

* minutes

Table 4 Product release tests that are common to both quality grades

TEST NAME	ENVIRONMENTAL TESTS TEST DESCRIPTION
Low air pressure (IEC 68-2-13)	25 °C/500 mbar/2 d
High pressure Leakage and seal line adhesive strength	60 °C/5 atm/1 hr 25 °C/freon/3 hrs

TEST NAME	MECHANICAL TESTS TEST DESCRIPTION
Vibration (IEC 68-2-6)	10-55 Hz/0.75 mm/2 hrs/side
Bump (IEC 68-2-29)	6 ms/40 g/1000x
Shock (IEC 68-2-27)	11 ms/100 g/3/side

ADDITIONAL TESTS FOR FIXED PINS	TEST DESCRIPTION
Sulpher dioxide (IEC 68-2-42)	25 °C/75% RH/25 ppm/10 d
Salt mist cyclic (IEC 68-2-52)	5% NaCl/3 d
Damp heat cyclic (IEC 68-2-30)	25-40 °C/90-95% RH/21 d

Note: d indicates days

RELIABILITY

Conditions for long life operation

A lifetime of 10^5 hours can be expected under normal operating conditions:

- operating voltage and frequency must be within the specified ranges
- DC voltage must be less than 0.1 V
- Operating ambient temperature range
  5 to 40 °C for commercial quality grade
  −5 to +55 °C for extended quality grade
- Relative humidity must be less than
  60% for commercial quality grade
  75% for extended quality grade

End of life definition

An LCD is considered to be at the end of its life if one of the following defects is found:

- optical or electro-optical defects
- electro-optical specifications are not met
- contrast lower than 50% of its initial value
- total current consumption at T_{amb} = 25 °C exceeds more than twice the specified maximum value
- the clearing point of the liquid crystal is less than the specified maximum operating ambient temperature

HANDLING ASPECTS

Unpacking

The instructions which are printed on the packaging should be followed.

Scratching

The front and rear sides of an LCD consist of polarizer and reflector foils. They are neither scratch nor pressure resistant, so avoid touching and treatment with rough or abrasive tools.

Fingerprints

Gloves should be worn when handling the displays as fingerprints on the polarizers can reduce the optical performance of the display and fingerprints on the contact sides can cause connecting problems.

Protective foil

Usually the front polarizer of a display is provided with a protective transparent foil (also the rear polarizer in transmissive mode LCDs). It should be kept in place as long as possible after the display has been removed from its original package, especially for temporary storage during manufacture. Ideally the protective foil should only be removed after the display is mounted in its final assembly. The foil can be removed using round ended tweezers with which it is lifted gently from a corner.

Cleaning

To clean a dirty LCD use a soft, clean, lint free, dry tissue. Loose dust may be removed by a clean, soft blower brush. If these methods are not sufficient then a tissue moistened with lead free benzine, petrol or freon and applied softly to the surface should be sufficient.
Other solvents or water have to be avoided as they may attack the polarizers.

Glass breakage

LCDs are made of glass. Handle with care to avoid breakage or cracks. If a display is broken use an alcohol- or acetone-soaked tissue to remove the escaped fluid. Avoid direct skin contact. Clean contaminated areas immediately with soap and warm running water.

Storage precautions

LCDs should be kept in their original package and in a dust-free environment for long term storage, temperature should not exceed 30 °C and relative humidity should not exceed 40 to 50%.
Avoid long term storage in direct sunlight: a yellow acryl box lends itself as a light, shock and dust protecting storage container.
Avoid moving a display from a cold storage area to a humid or hot storage area as it leads to condensation which can attack the polarizers.

MOUNTING ASPECTS

Housing

Housing and frame dimensions should be well adapted to the size of the display to assure proper mounting. Mechanical pressure should be moderate and should be applied evenly between the frame and the full length of the display. No pressure should be exerted on the seal or on the display areas.
Module housings and frames have to be designed in such a way that bending of a display in the mounted position is minimized.
LCDs should preferably be housed with a transparent plate (e.g. glass or non-birefringent acrylic plate) mounted in front of the display to protect it from scratches, humidity and dirt.

Conductive rubber connections

Mounting instructions from the manufacturers of elastomeric connectors (conductive rubber "zebra") have to be followed. Special attention should be given to the prescribed contact pressure and its even spread over the full length of the contacting edges.

Soldering

When soldering LCDs with fixed-pins, avoid temperature shocks. If using solder-wave equipment with preheating it may be necessary to cover the LCD to avoid exceeding the maximum storage temperature.
As LCDs should not be washed, we recommend that the protective foil be left in place until after soldering as it helps to protect the display from solder flux splashes. Additional protection may be required.

Custom design

Custom design

INTRODUCTION TO CUSTOM DESIGN

The advantage of LCD technology over many other display technologies is the capability of supplying LCDs to specific customer requirements.

We offer a complete custom design service for LCD cells in which the following aspects can be customer specified:

- dimensions
- display pattern
- electro-optical characteristics
- connection methods

Our custom design facility has been divided into two categories: **semi-standard** products and **custom** products. Each category has different priorities on design flexibility versus development time and development cost.

Semi-standard products are a custom designed display pattern incorporated with a variety of standard options, which include a range of standard glass sizes and a selection of electro-optical characteristics. As a result, **semi-standard** products require only a simple product definition, have a fast development time and a low development cost.

Custom products offer much more flexibility in dimensions and electro-optical characteristics but should only be specified when **semi-standard** product options do not meet with customer requirements.

Customers wishing to order a custom design product or who require more information should contact our sales representative (see back of handbook for the address).

DEVELOPMENT PROCEDURE

Custom design projects consist of three main stages:

- product definition and quotation
- sample phase
- volume production

Product definition and quotation

In this phase our development department translates the customers requirements into a product specification (electro-optical characteristics and product drawing). This specification will enable assessment and will be offered to the customer as a part of the final commercial quotation.

Sample phase

Once the final quotation has been accepted samples of the product will be made according to the agreed specification. The customer will be required to give formal approval of the samples prior to the volume production phase.

Volume production

Preparations for volume production will begin once sample approval has been gained and deliveries will begin after a specified lead time.

SEMI-STANDARD PRODUCTS

Features

With semi-standard products we offer a custom design facility that provides:

- low development costs
- short design time
- a wide range of standard glass sizes
- a choice of electro-optical specifications
- cells for conductive rubber (elastomer) or with fixed-pin connectors
- easy product definition by means of a simple order form (see tear out sheet at the back of this handbook)

Ratings

Maximum voltage between any two contacts	V_{max}	15 V rms 0.1 V DC
Storage temperature		
For commercial quality grade	T_{stg}	−25 to +70 °C
For extended quality grade	T_{stg}	−40 to +90 °C

Mechanical data

Table 5 is a list of available semi-standard glass sizes, it contains that data which is size dependant.

Table 6 contains the data that is common to all semi-standard glass sizes.

Four basic outline versions are available: a, b, c and d (as specified in Figs 28, 29, 30 and 31).

A wider range of mechanical data is available in the category **Custom Products.**

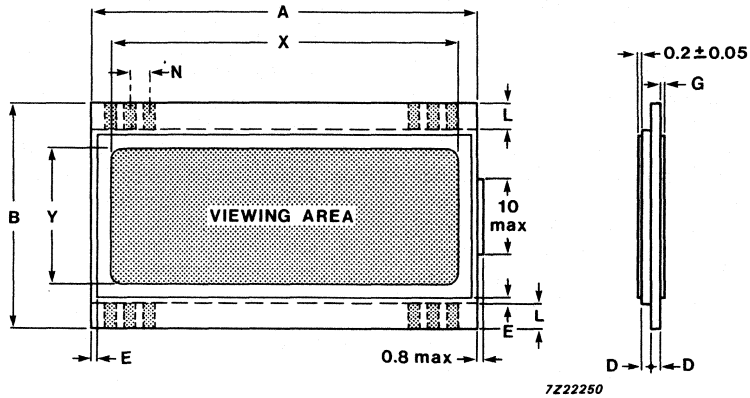


Fig.28 Version a, for conductive rubber connection, contacts top and bottom.

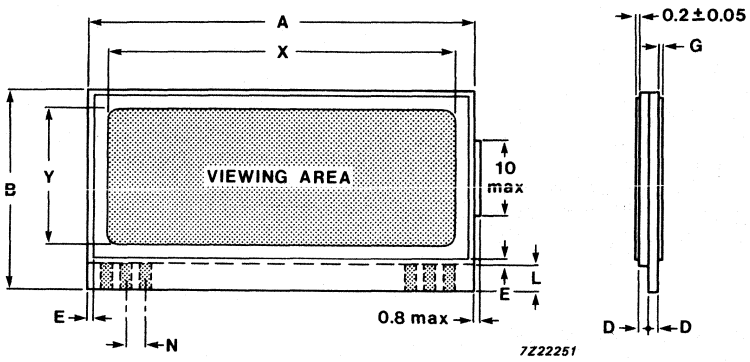


Fig.29 Version b, for conductive rubber connection, contacts bottom only.

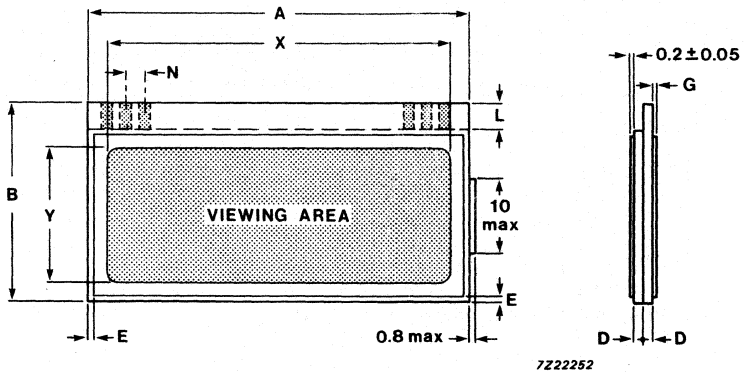
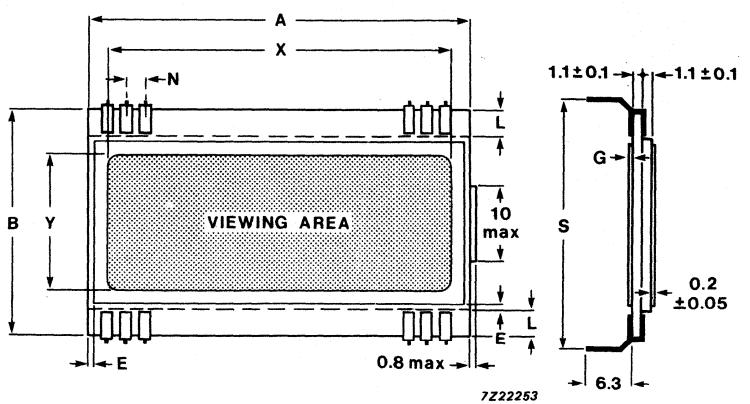


Fig.30 Version c, for conductive rubber connection, contacts top only.



N = 2.54 mm

Fig.31 Version d, with fixed pins, top and bottom.

Dimensions A, B and L are nominal values. Their tolerance is dependent upon glass thickness D, when D = 1.1 mm, tolerance = ± 0.25 mm and when D = 0.7 mm, tolerance = 0.2 mm.
Dimensions X and Y are minimum values.

Table 5 Main dimensions for semi-standard glass sizes

SIZE ID.		DIMENSIONS					NUMBER OF AVAILABLE CONTACTS			
REF. AVAILABLE VERSIONS (1)		A mm	B mm	L mm	X mm	Y mm	NOT FIXED-PIN VERSION D N = 1.0 mm	N = 1.27 mm	N = 1.8 mm	N = 2.54 mm
S 380	a, d	37.6	19.5	2.55	32.6	10.4	2 X 36	2 X 28	2 X 20	2 X 14
S 381	a, d	37.6	21.9	2.55	32.6	12.8	2 X 36	2 X 28	2 X 20	2 X 14
S 382	a	38.1	22.0	1.7	34.1	14.6	2 X 36	2 X 29	2 X 20	2 X 14
S 400	b, c	40.0	20.0	2.0	36.0	14.0	1 X 38	1 X 30	1 X 21	1 X 15
S 430	b, c	42.9	20.9	2.55	37.9	14.3	1 X 41	1 X 33	1 X 23	1 X 16
S 500	a, d	50.1	19.5	2.55	45.1	10.4	2 X 48	2 X 38	2 X 27	2 X 19
S 501	a, d	50.1	29.7	2.55	45.1	20.6	2 X 48	2 X 38	2 X 27	2 X 19
S 510	a, d	50.8	30.4	2.55	45.8	20.3	2 X 49	2 X 39	2 X 27	2 X 20
S 511	a, d	50.8	80.0	3.8	45.8	67.4	2 X 49	2 X 39	2 X 27	2 X 20
S 520	b, c	52.0	22.0	3.0	48.0	15.0	1 X 50	1 X 40	1 X 28	1 X 20
S 700	a, d	69.8	20.3	2.55	65.8	11.2	2 X 68	2 X 54	2 X 38	2 X 27
S 701	a, d	69.8	30.4	2.55	64.8	20.3	2 X 68	2 X 54	2 X 38	2 X 27
S 702	a, d	69.8	38.0	3.8	64.8	25.4	2 X 68	2 X 54	2 X 38	2 X 27
S 750	a, d	75.1	29.7	2.55	70.1	20.6	2 X 73	2 X 58	2 X 41	2 X 29
S 810	a, d	81.1	38.0	3.8	76.1	25.4	2 X 79	2 X 63	2 X 44	2 X 31
S 940	a, d	93.8	30.4	3.8	88.8	17.8	2 X 92	2 X 73	2 X 51	2 X 36
S 941	a, d	93.8	38.0	3.8	88.8	25.4	2 X 92	2 X 73	2 X 51	2 X 36
S 942	a, d	93.8	46.0	3.8	88.8	33.4	2 X 92	2 X 73	2 X 51	2 X 36
S 1000	a, d	100.1	25.2	2.55	94.1	15.1	2 X 98	2 X 78	2 X 55	2 X 39
S 1140	a, d	114.0	26.0	2.55	109.0	15.9	2 X 112	2 X 89	2 X 63	2 X 44
S 1141	a, d	114.0	46.0	3.8	109.0	33.4	2 X 112	2 X 89	2 X 63	2 X 44
S 1500	a, d	150.1	47.9	2.55	144.1	37.8	2 X 148	2 X 117	2 X 83	2 X 58

Note: when refering to a specific glass size state its reference and version number e.g. S 510-a.

(1) for version: a see Fig.28
b see Fig.29
c see Fig.30
d see Fig.31

Table 6 Other dimensions for semi-standard glass sizes

If more than one nominal value is stated the customer has a free choice of one of the values, unless otherwise specified.

DESCRIPTION	DIMENSION	NOMINAL VALUE (mm)	TOLERANCE ± (mm)
glass thickness	D	1.1	0.1
	D	0.7	0.1
rear polarizer thickness			
– reflective or transflective	G	0.3	0.05
– transmissive	G	0.2	0.05
pitch of contacts for conductive rubber connection	N	1.0	– (1)
	N	1.27	– (1)
	N	1.8	– (1)
	N	2.54	– (1)
width of contact for conductive rubber connection			
– for N = 1.0 mm		0.5	–
– for N = 1.27 mm		0.6	–
– for N = 1.8 mm		0.9	–
– for N = 2.54 mm		1.5	–

(1) Accumulated tolerance over the complete row of contacts = 0.1 mm.

Display pattern and terminal connections

Technical conditions for acceptance as semi-standard product:

The total number of display segments should not exceed 120.

The selected glass size should have enough connections to accommodate the required number of display segments at the chosen multiplex rate.

Backplane contacts must be located in the corners with a maximum of 2 per corner.

Available letter types

- Akzidenz-grotesk stnd
- Eurostyle bold
- Futura bold italic
- Helvetica medium
- Helvetica medium condensed
- Helvetica medium italic
- Univers 57
- Univers 67
- Univers 68
- Univers 75

Note: final technical acceptance is made by our design department, who will determine if design, within our design rules is possible.

Terminal connections

If a symbol occurs more than once within a multiplexed LCD our development department will use the same segment-to-backplane assignment; this standard procedure simplifies the driver software because only one look-up table is required.

As LCD technology allows only single layer interconnection tracks, customer requirements on segment to backplane assignment and on terminal connections may collide with LCD track routing restrictions. In order to obtain optimal LCD design and thereby optimal optical appearance the customer is advised to specify only minimum requirements on these aspects. If any additional requirements or preferences are indicated separately, our design department will advise on these matters.

Pattern dimensions

Minimum distance between segments without leads in between	
– both segments relating to the same backplane	0.2 mm
– both segments relating to a different backplane	0.3 mm
– with one lead in between	0.35 mm
Minimum distance between symbols depends upon the number of leads between the symbols	
Minimum distance between segments and viewing area border	1.0 mm
Positional tolerance of graphic elements with respect to each other	±0.1 mm
Tolerance of graphics in relation to nominal glass edge position	±0.2 mm

Characteristics

A range of 8 different specifications are available as described in the chapter "General LCD Family Characteristics".

Table 7 Quick reference survey

PAR.	SYMB.	FAMILY CHARACTERISTICS								UNIT
		TR1, TF1, TU1				TR2, TF2, TU2			TR3, TF3, TU3	
drive method	–	DD	1:2	1:3	1:4	DD	1:3	1:4	1:2	
operating voltage	V_{op}	2.5–6	2.8	3.1	3.2	3–6	4.3	4.5	5	V
ambient op. temp. min.	T_{amb}	−10	−10	−10	−10	−25	−25	−20	−25	°C
max.	T_{amb}	60	50	50	40	80	60	50	80	°C
quality grade	–	commercial				extended			extended	

Optical description

Table 8 Survey of optical descriptions

PARAMETER	FAMILY CHARACTERISTICS		
	TR1, TR2, TR3	TF1, TF2, TF3	TU1, TU2, TU3
image mode	positive	positive	negative
illumination mode	reflective	transflective	transmissive
antiglare surface	no	no	yes

Preferred viewing direction $\varphi_{pref} = 90°$ or $\varphi_{pref} = 270°$ (see Fig.32)

Position of contact sides $\varphi = 0°/180°$ (see Fig.32)

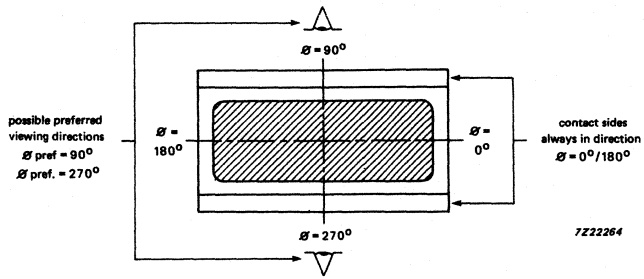


Fig.32 Preferred viewing direction in relation to contact sides, for semi-standard products.

Note: a wider choice of preferred viewing directions and contact side positions is available for **Custom products.**

CUSTOM PRODUCTS

In this product category we offer LCD cells with dimensions according to customer specifications and a variety of electro-optical specifications.

In this section only concise information can be given as much depends upon customer requirements.

Those customers requiring more information should contact our sales representative (see back of handbook for address).

Mechanical data

Custom products can be tailor-made to any size which is within specified design rules. However, certain dimensions, like those specified for semi-standard products, will lead to optimal production efficiency and will thereby result in cost effective solutions.

Custom products are available in two glass thicknesses:
0.7 mm ± 0.1 mm or
1.1 mm ± 0.1 mm

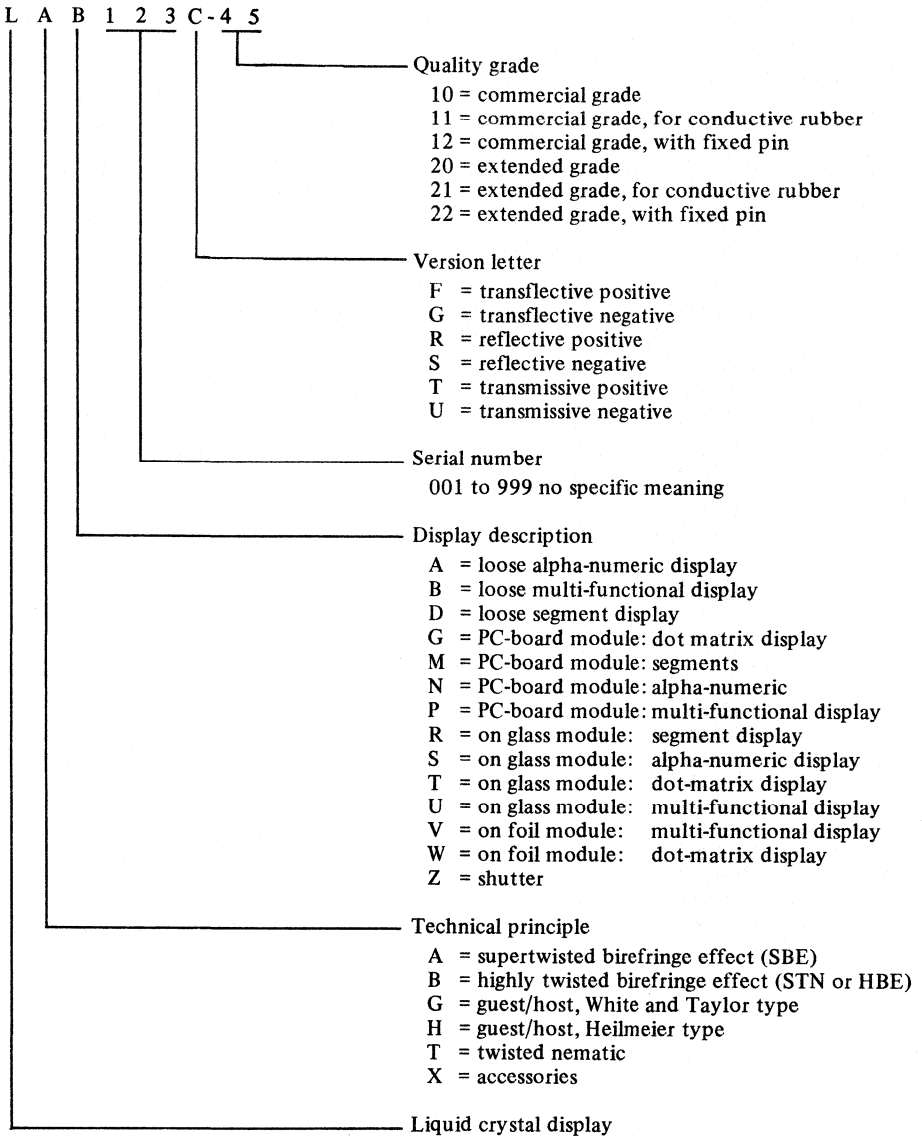
Electro-optical specifications

There are a wide range of specifications available which include those given in the chapter "Family Characteristics". They include specifications for applications requiring different drive voltages, optical specifications etc.

Type code information

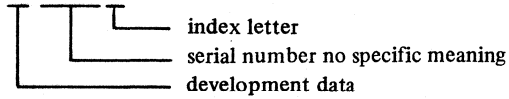
page

TYPE NUMBER DESIGNATIONS



TYPE NUMBERS FOR DEVELOPMENT DATA

LP-XXXX-I



CROSS REFERENCE GUIDE

OLD TYPE NO.	NEW TYPE NO.
LC241440-101	LTD201
LC283020-301	LTD202
LC382040-401	LTD203
LC382080-411	LTD211
LC512332-300	LTD101
LC513031-300	LTD221
LC513031-302	LTD222
LC513031-303	LTD222
LC513031-307	LTD224
LC513031-309	LTD221
LC513031-320	LTD231
LC513031-390	LTD225
LC513040-301	LTD226
LC513040-303	LTD226
LC513041-300	LTD227
LC513041-320	LTD232
LC513050-300	LTD228
LC518000-301	LTA141
LC554731-312	LTD132
LC7020160-412	LTD233
LC7020160-430	LTD234
LC703000-300	LTD321
LC703060-301	LTD229
LC703831-300	LTD241
LC703840-300	LTD242
LC07610110-300	LTD261
LC943080-301	LTD262
LC943860-301	LTD263
LC11402600-310	LTD351
LC11404650-301	LTD264
MB 70 20 160	LTM233

General LCD family characteristics

Family characteristics

FAMILY CHARACTERISTICS

Standard range LCD cells are offered in two quality grades: commercial (over the commercial temperature range) and extended (over the extended temperature range). The following chapter contains the variations in operating characteristics for the two grades in the three illumination modes.

TR0, TF0

Optical description

	ILLUMINATION MODE	IMAGE MODE	FRONT SURFACE
TR0	reflective	positive	glossy
TF0	transflective	positive	glossy

Quality grade: commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; V_{op} = $V_{op\ typ}$; f_{dr} = 32 Hz unless otherwise specified

PARAMETER	SYMBOL		DRIVE METHOD DD*	UNIT	NOTE
operating voltage	V_{op}	min.	3.0	V	(1)
		typ.	4.5	V	
		max.	6.0	V	
operating ambient temperature	T_{amb}	min.	−10	°C	
		max.	+60	°C	
turn-on time at					
T_{amb} = 25 °C		t_{on}	40	ms	(2)
T_{amb} = 0 °C		t_{on}	200	ms	
turn-off time at					
T_{amb} = 25 °C		t_{off}	80	ms	(2)
T_{amb} = 0 °C		t_{off}	150	ms	
specific capacitance	C_S		11	pF/mm²	
specific current consumption	I_S		10	nA/mm²	
frame frequency	f_{dr}	min.	30	Hz	(1)
		max.	200	Hz	

* DD = direct drive

(1) For definition see Fig.33.
(2) For definition see Fig.34.

TR1, TF1, TU1

Optical description

	ILLUMINATION MODE	IMAGE MODE	FRONT SURFACE
TR1	reflective	positive	glossy
TF1	transflective	positive	glossy
TU1	transmissive	negative	antiglare

Quality grade: commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; V_{op} = $V_{op\ typ}$; f_{dr} = 32 Hz unless otherwise specified

PARAMETER	SYMBOL		DRIVE METHOD				UNIT	NOTE
			DD*	1:2	1:3	1:4		
operating voltage	V_{op}	min.	2.5	–	–	–	V	(1)
		typ.	4.5	2.8	3.1	3.2	V	
		max.	6.0	–	–	–	V	
operating ambient temperature	T_{amb}	min.	−10	−10	−10	−10	°C	
		max.	+60	+50	+50	+40	°C	
turn-on time at								
T_{amb} = 25 °C		t_{on}	50	150	180	160	ms	(2)
T_{amb} = 0 °C		t_{on}	250	1000	1200	1400	ms	
turn-off time at								
T_{amb} = 25 °C		t_{off}	90	90	60	75	ms	(2)
T_{amb} = 0 °C		t_{off}	400	300	300	300	ms	
specific capacitance	C_s		15	15	15	15	pF/mm²	
specific current consumption	I_s		15	15	22	22	nA/mm²	
frame frequency	f_{dr}	min.	30	30	30	30	Hz	(1)
		max.	200	100	100	100	Hz	

* DD = direct drive

(1) For definition see Fig.33.
(2) For definition see Fig.34.

Electro-optical characteristics for temperature-compensated drive voltage **TR1, TF1, TU1**
Typical values at T_{amb} = 25 °C; $V_{op} = V_{op\ typ} + TC \cdot T_{amb}$; f_{dr} = 32 Hz unless otherwise specified

PARAMETER	SYMBOL		DRIVE METHOD			UNIT	NOTE
			1:2	1:3	1:4		
operating voltage	V_{op}	typ.	3.1	3.3	3.3	V	(1)
temperature coefficient of V_{op}	TC		−13	−14	−14	mV/K	
operating ambient temperature range	T_{amb}	min.	−10	−10	−10	°C	
		max.	+60	+60	+60	°C	
turn-on time at							
T_{amb} = 25 °C	t_{on}		80	120	140	ms	(2)
T_{amb} = 0 °C	t_{on}		350	700	850	ms	
turn-off time at							
T_{amb} = 25 °C	t_{off}		90	80	80	ms	(2)
T_{amb} = 0 °C	t_{off}		450	350	350	ms	
frame frequency	f_{dr}	min.	30	30	30	Hz	(1)
		max.	100	100	100	Hz	

(1) For definition see Fig.33.
(2) For definition see Fig.34.

TR2, TF2, TU2

Optical description

	ILLUMINATION MODE	IMAGE MODE	FRONT SURFACE
TR2	reflective	positive	glossy
TF2	transflective	positive	glossy
TU2	transmissive	negative	antiglare

Quality grade: extended

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; V_{op} = $V_{op\ typ}$; f_{dr} = 32 Hz unless otherwise specified

PARAMETER	SYMBOL		DRIVE METHOD				UNIT	NOTE
			DD*	1:2	1:3	1:4		
operating voltage	V_{op}	min.	3.0	–	–	–	V	(1)
		typ.	4.5	3.9	4.4	4.5	V	
		max.	6.0	–	–	–	V	
operating ambient temperature	T_{amb}	min.	−25	−25	−25	−20	°C	
		max.	+80	+80	+50	+50	°C	
turn-on time at								
T_{amb} = 25 °C		t_{on}	40	75	90	100	ms	(2)
T_{amb} = 0 °C		t_{on}	200	300	450	500	ms	
turn-off time at								
T_{amb} = 25 °C		t_{off}	80	40	50	40	ms	(2)
T_{amb} = 0 °C		t_{off}	150	180	110	150	ms	
specific capacitance	C_S		11	11	11	11	pF/mm²	
specific current consumption	I_S		10	10	15	15	nA/mm²	
frame frequency	f_{dr}	min.	30	30	30	30	Hz	(1)
		max.	200	100	100	100	Hz	

* DD = direct drive

(1) For definition see Fig.33.
(2) For definition see Fig.34.

Electro-optical characteristics for temperature-compensated drive voltage **TR2, TF2, TU2**

Typical values at T_{amb} = 25 °C; V_{op} = $V_{op\ typ}$ + TC • T_{amb}; f_{dr} = 32 Hz unless otherwise specified

PARAMETER	SYMBOL		DRIVE METHOD 1:2	DRIVE METHOD 1:3	DRIVE METHOD 1:4	UNIT	NOTE
operating voltage	V_{op}	typ.	4.3	4.6	4.6	V	(1)
temperature coefficient of V_{op}	TC		−13	−14	−14	mV/K	
operating ambient temperature range	T_{amb}	min.	−25	−25	−25	°C	
		max.	+80	+80	+80	°C	
turn-on time at							
T_{amb} = 25 °C	t_{on}		40	60	80	ms	(2)
T_{amb} = 0 °C	t_{on}		150	250	350	ms	
turn-off time at							
T_{amb} = 25 °C	t_{off}		50	50	50	ms	(2)
T_{amb} = 0 °C	t_{off}		200	180	200	ms	
frame frequency	f_{dr}	min.	30	30	30	Hz	(1)
		max.	100	100	100	Hz	

(1) For definition see Fig.33.
(2) For definition see Fig.34.

TR3, TF3, TU3

Optical description

	ILLUMINATION MODE	IMAGE MODE	FRONT SURFACE
TR3	reflective	positive	glossy
TF3	transflective	positive	glossy
TU3	transmissive	negative	antiglare

Quality grade: commercial

Electro-optical characteristics for constant drive voltage

Typical values at T_{amb} = 25 °C; V_{op} = $V_{op\ typ}$; f_{dr} = 32 Hz unless otherwise specified

PARAMETER	SYMBOL		DRIVE METHOD				UNIT	NOTE
			DD*	1:2	1:3	1:4		
operating voltage	V_{op}	typ.	–	5.0	–	–	V	(1)
operating ambient temperature	T_{amb}	min.	–	−25	–	–	°C	
		max.	–	80	–	–	°C	
turn-on time at								
T_{amb} = 25 °C		t_{on}	–	95	–	–	ms	(2)
T_{amb} = 0 °C		t_{on}	–	310	–	–	ms	
turn-off time at								
T_{amb} = 25 °C		t_{off}	–	35	–	–	ms	(2)
T_{amb} = 0 °C		t_{off}	–	90	–	–	ms	
specific capacitance	C_s		–	15	–	–	pF/mm²	
specific current consumption	I_s		–	10	–	–	nA/mm²	
frame frequency	f_{dr}	min.	–	30	–	–	Hz	(1)
		max.	–	100	–	–	Hz	

* DD = direct drive

(1) For definition see Fig.33.
(2) For definition see Fig.34.

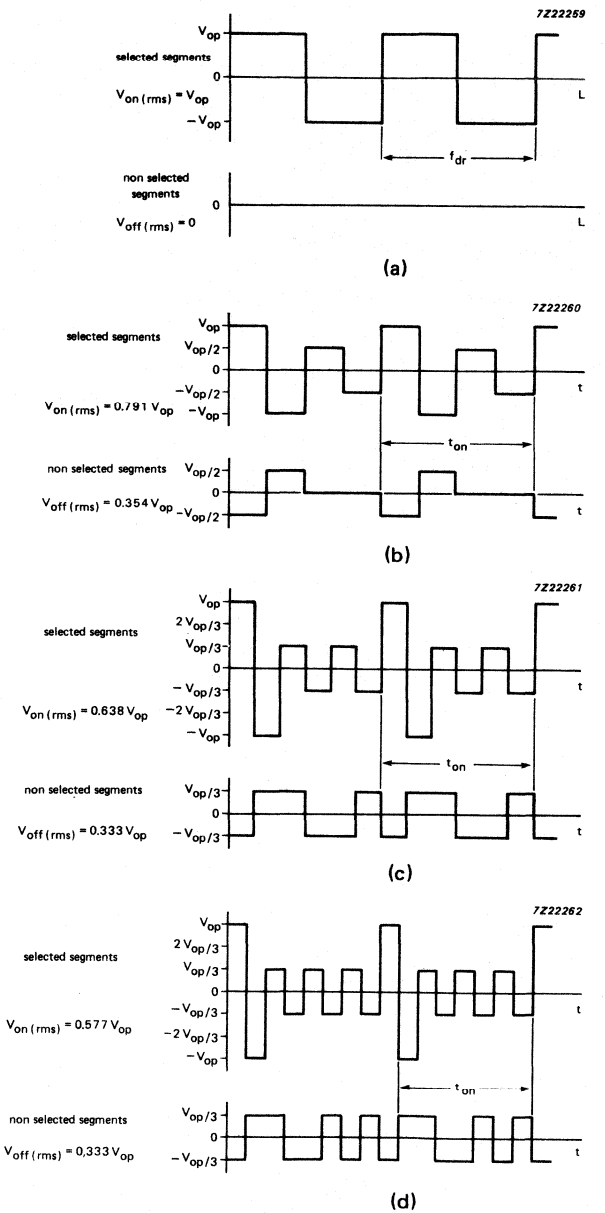
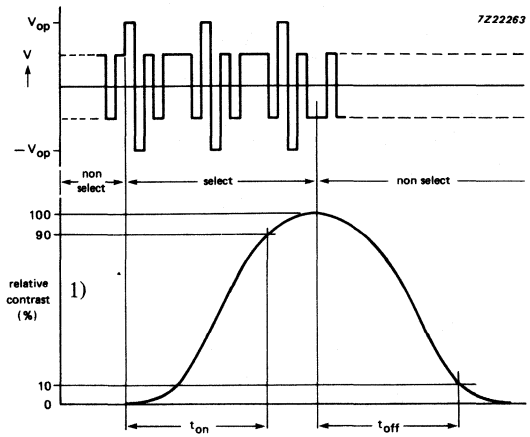


Fig.33 Typical V_{op} waveforms
(a) direct drive (b) MUX 1:2 (c) MUX 1:3
(d) MUX 1:4.



1) measured perpendicular to the display.

Fig.34 Definition of response times.

LCD cell data

NOTES TO CELL DATA MECHANICAL DRAWINGS

A number of details have been omitted from the drawings given under the "Mechanical Data" of this section. We have provided the missing data below and apologise for the inconvenience.

1. Preferred viewing direction

Please refer to the *Quick reference data* of the data sheet.

2. Segment designations

Please refer to Fig.35.

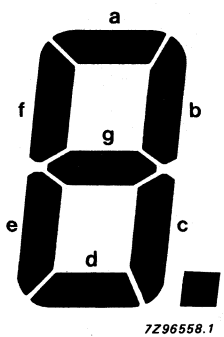


Fig.35 Segment designations

3. Tolerances

Tolerance on glass thickness = ±0.1mm

Tolerance on outer glass dimensions

+0.4/−0.2 mm for:	LTD222/226/227/229/241/242/261/262/264/351 LP-2703
±0.25 mm for:	LTA141, LTD202/221/224/225/228/231/232/263/321
±0.2 MM for:	LTD101/132/201/203/211/233/234

Liquid crystal display LP-2703

DEVICE DESCRIPTION

The LP-2703-B is a 3½-digit 7 segment clock display with AM and PM functions. It is designed for use with the PCF1175 clock circuit.

QUICK REFERENCE DATA

Viewing area dimensions	32.5 X 14.1 mm
Overall glass dimensions	37.5 X 20.8 mm
Thickness	1.9 ± 0.2 mm
Digit height	8.5 mm
Preferred viewing direction	12 o'clock
Driving method	MUX 1:2
Operating voltage V_{op}	5 V

DISPLAY MODE

Scale 1:1

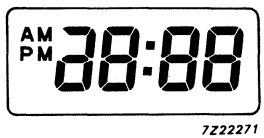


Fig.1 Clock display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LP-2703-B	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.

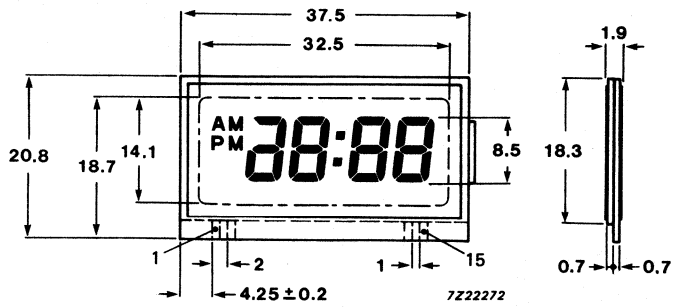


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	SEGMENT ASSIGNED TO COMMON 2
1	comm 1	–
2	–	comm 2
3	AM	PM
4	a2	adeg1
5	b1	c1
6	f2	e2
7	g2	d2
8	b2	c2
9	a4	co1
10	f3	e3
11	g3	ad3
12	b3	c3
13	f4	e4
14	g4	d4
15	b4	c4

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	10 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, multiplex drive 1:2

TYPE	FAMILY CHARACTERISTICS
LP-2703-B	TR3

Liquid crystal display LTA141

DEVICE DESCRIPTION

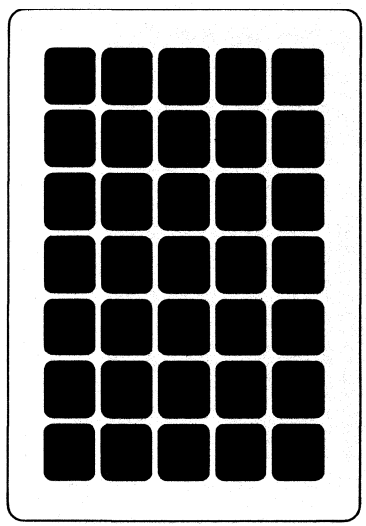
The LTA141R;F is a single character display of 5 X 7 dots. Typical applications include communications panels for air terminals.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 X 67.4 mm
Overall glass dimensions	50.8 X 80.0 mm
Thickness	2.7 ± 0.3 mm
Digit height	37.2 X 57.3 mm
Preferred viewing direction	12 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1



7Z22323

Fig.1 Universal display.

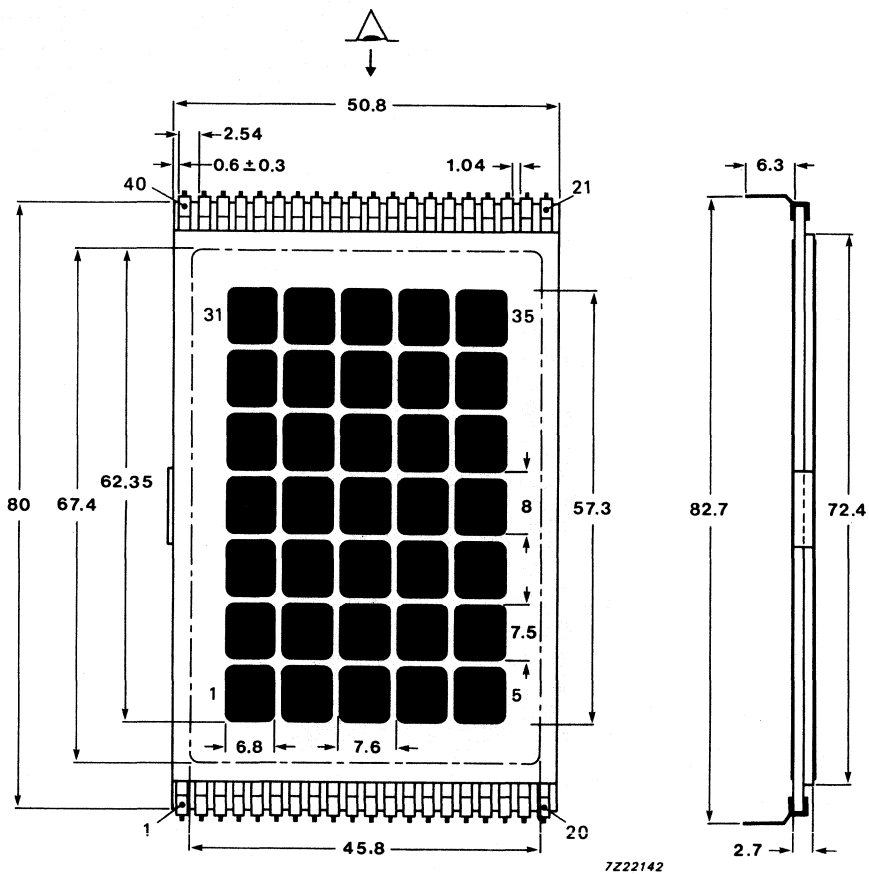
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTA141R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTA141F-12	transflective	with fixed pin	−10 to 60 °C	commercial
LTA141R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTA141F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred driver: PCF8576

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON
1	comm
2	
3	
4	
5	1
6	10
7	12
8	2
9	9
10	8
11	3
12	13
13	7
14	4
15	14
16	17
17	5
18	6
19	15
20	nc

PIN NO.	SEGMENT ASSIGNED TO COMMON
21	16
22	25
23	26
24	35
25	24
26	27
27	34
28	23
29	28
30	33
31	18
32	19
33	32
34	29
35	22
36	31
37	30
38	21
39	20
40	11

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections — V_{max} — 15 V rms / 0.1 V DC

Storage temperature range

LTA141R-12, LTA141F-12 — T_{stg} — −25 to +70 °C

LTA141R-22, LTA141F-22 — T_{stg} — −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTA141R-12	TR0
LTA141F-12	TF0
LTA141R-22	TR2
LTA141F-22	TF2

Liquid crystal display LTD101

DEVICE DESCRIPTION

The LTD101R-11 is a 3 ½-digit, 7-segment clock LCD with AM and PM functions. It is intended for use in small alarm clocks in either 12 hr. or 24 hr. mode.

QUICK REFERENCE DATA

Viewing area dimensions	46.4 X 13.4 mm
Overall glass dimensions	50.8 X 22.9 mm
Thickness	2.7 ± 0.4 mm
Digit height	8.9 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

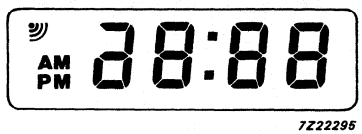


Fig.1 Clock display.

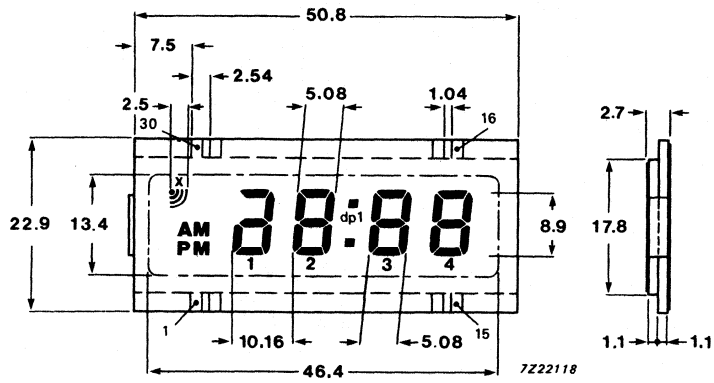
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD101R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Clock driver: PCF1171, PCF1172, PCF1174
Preferred drivers: PCF2112, PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	nc
2	comm
3	PM
4	a1, b1, d1, e1
5	c1
6	e2
7	d2
8	c2
9	dp1
10	e3
11	d3
12	c3
13	e4
14	d4
15	c4

PIN NO.	SEGMENT
16	b4
17	a4
18	f4
19	g4
20	b3
21	a3
22	f3
23	g3
24	b2
25	a2
26	f2
27	g2
28	b1
29	AM
30	X

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD101R-11	TR0

Liquid crystal display LTD132

DEVICE DESCRIPTION

The LTD132R-11 is a 3 ½-digit, 7-segment clock LCD intended for use in alarm clocks with 12 hrs mode. It can be driven by an MSM5015 clock circuit.

QUICK REFERENCE DATA

Viewing area dimensions	38.0 X 49.8 mm
Overall glass dimensions	46.8 X 54.8 mm
Thickness	2.7 ± 0.4 mm
Digit height	5.6 mm
Preferred viewing direction	12 o'clock
Driving method	MUX 1:2
Operating voltage V_{op}	2.8 to 3.2 V

DISPLAY MODE

Scale 1:1

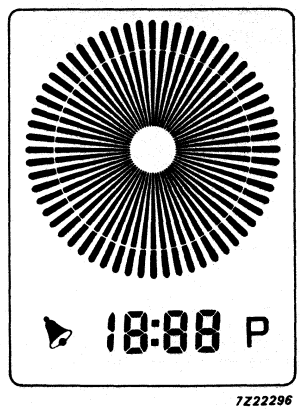


Fig.1 Analogue clock display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD132R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Unused segments to be controlled "off".

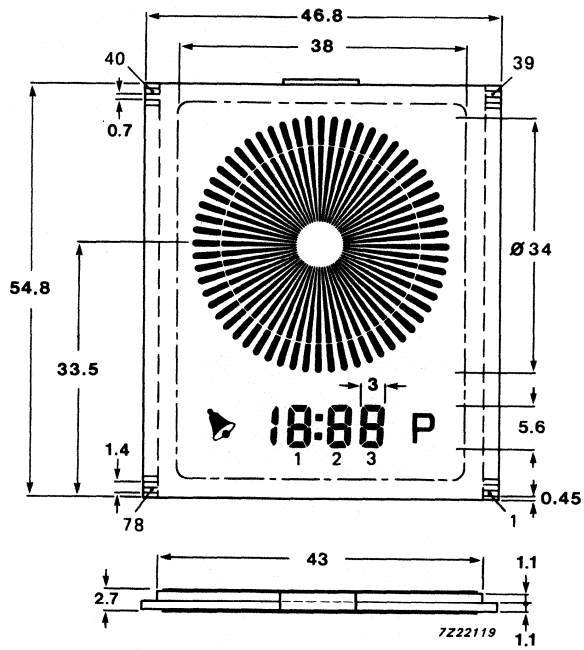


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2
1	f2	e2
2	comm 1	
3	a2d2	g2
4	b2	c2
5	f3	e3
6	g3	d3
7	b3	c3
8	P	
9	a3	DP1/2
10	X29	Y29
11	X28	Y28
12	X27	Y27
13	X26	Y26
14	X25	Y25
15	X24	Y24
16	X23	Y23
17	X22	Y22
18	X21	Y21
19	X20	Y20
20	X19	Y19
21	X18	Y18
22	X17	Y17
23	X16	Y16
24	X15	Y15
25	X14	Y14
26	X13	Y13
27	X12	Y12
28	X11	Y11
29	X10	Y10
30	X9	Y9
31	X8	Y8
32	X7	Y7
33	X6	Y6
34	X5	Y5
35	X4	Y4
36	X3	Y3
37	X2	Y2
38	comm 1	
39	X1	Y1

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2
40		comm 2
41	X60	Y60
42	X59	Y59
43	X58	Y58
44	X57	Y57
45	X56	Y56
46	X55	Y55
47	X54	Y54
48	X53	Y53
49	X52	Y52
50	X51	Y51
51	X50	Y50
52	X49	Y49
53	X48	Y48
54	X47	Y47
55	X46	Y46
56	X45	Y45
57	X44	Y44
58	X43	Y43
59	X42	Y42
60	X41	Y41
61	X40	Y40
62	X39	Y39
63	X38	Y38
64	X37	Y37
65	X36	Y36
66	X35	Y35
67	X34	Y34
68	X33	Y33
69	X32	Y32
70	X31	Y31
71	X30	Y30
72		AL
73	a1	h
74	f1	e1
75	g1	d1
76	b1	c1
77		comm 2
78	NC	NC

Preferred driver: MSM5015

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, multiplex drive 1:2

TYPE	FAMILY CHARACTERISTICS
LTD132R-11	TR1

Liquid crystal display LTD201

DEVICE DESCRIPTION

The LTD201R-11 is a 4-digit, 7-segment LCD. It is intended for applications requiring a very small display.

QUICK REFERENCE DATA

Viewing area dimensions	21.5 × 9.4 mm
Overall glass dimensions	23.9 × 14,0 mm
Thickness	1.6 ± 0.2 mm
Digit height	6.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

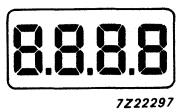


Fig.1 Universal display.

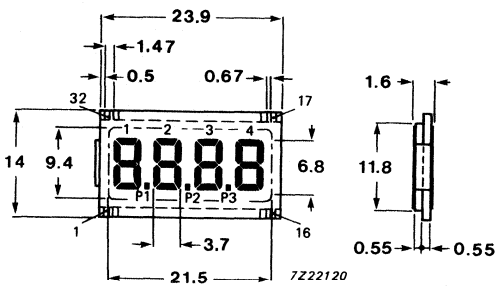
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD201R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112, PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	e1
3	d1
4	c1
5	p1
6	e2
7	d2
8	c2
9	p2
10	e3
11	d3
12	c3
13	p3
14	e4
15	d4
16	c4

PIN NO.	SEGMENT
17	b4
18	a4
19	f4
20	g4
21	b3
22	a3
23	f3
24	g3
25	b2
26	a2
27	f2
28	g2
29	b1
30	a1
31	f1
32	g1

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD201R-11	TR0

Liquid crystal display LTD202

DEVICE DESCRIPTION

The LTD202R;F is a 2-digit, 7-segment LCD. It is intended for application in small counters and indicator panels.

QUICK REFERENCE DATA

Viewing area dimensions	23.5 X 18.4 mm
Overall glass dimensions	27.9 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

Fig.1 Universal display.

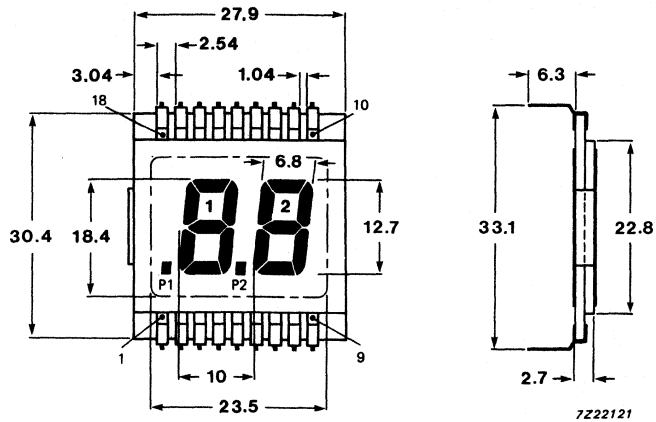
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD202R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTD202R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD202F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF8577, PCF2112

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	p2
3	e2
4	d2
5	c2
6	p1
7	e1
8	d1
9	c1

PIN NO.	SEGMENT
10	b1
11	a1
12	f1
13	g1
14	b2
15	a2
16	f2
17	g2
18	nc

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range LTD202R-12 LTD202R-22, LTD202F-22	T_{stg}	 −25 to +70 °C −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD202R-12	TR0
LTD202R-22	TR2
LTD202F-22	TF2

Liquid crystal display LTD203

DEVICE DESCRIPTION

The LTD203R;F is a 4-digit, 7-segment multi-function LCD. Typical applications include counters, multi-meters and 24 hr. clocks.

QUICK REFERENCE DATA

Viewing area dimensions	34.0 X 11.2 mm
Overall glass dimensions	38.0 X 20.3 mm
Thickness	2.2 ± 0.4 mm
Digit height	8.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

Fig.1 Universal display.

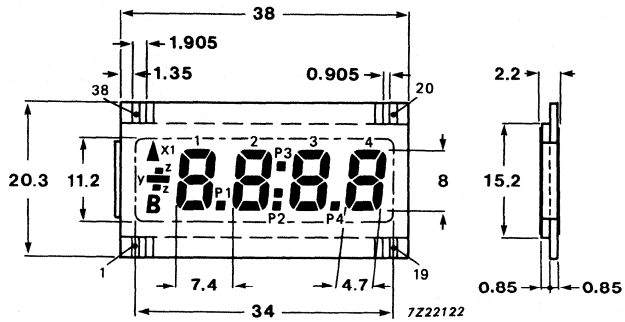
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD203R-11	reflective	for conductive rubber	−10 to 60 °C	commercial
LTD203R-21	reflective	for conductive rubber	−25 to 80 °C	extended
LTD202F-21	transflective	for conductive rubber	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112, PCF8576

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	B
3	e1
4	d1
5	c1
6	p1
7	e2
8	d2
9	c2
10	p2
11	e3
12	d3
13	c3
14	p4
15	e4
16	d4
17	c4
18	g4
19	nc

PIN NO.	SEGMENT
20	b4
21	a4
22	f4
23	g3
24	b3
25	a3
26	f3
27	p3
28	g2
29	b2
30	a2
31	f2
32	g1
33	b1
34	a1
35	f1
36	y
37	z
38	X1

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range LTD203R-11 LTD203R-21, LTD203F-21	T_{stg}	 −25 to +70 °C −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD203R-11	TR0
LTD203R-21	TR2
LTD203F-21	TF2

Liquid crystal display LTD211

DEVICE DESCRIPTION

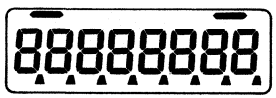
The LTD211R;F is an 8-digit, 7-segment multi-function display. Typical applications include cordless telephones and industrial instruments.

QUICK REFERENCE DATA

Viewing area dimensions	34.0 X 11.2 mm
Overall glass dimensions	38.0 X 20.3 mm
Thickness	2.2 ± 0.4 mm
Digit height	6.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:2
Operating voltage V_{op}	2.8 V

DISPLAY MODE

Scale 1:1



7Z22300

Fig.1 Telecom display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD211R-11	reflective	for conductive rubber	−10 to 60 °C	commercial
LTD211F-11	transflective	for conductive rubber	−10 to 60 °C	commercial
LTD211R-21	reflective	for conductive rubber	−25 to 80 °C	extended
LTD211F-21	transflective	for conductive rubber	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Unused segments to be controlled "off".

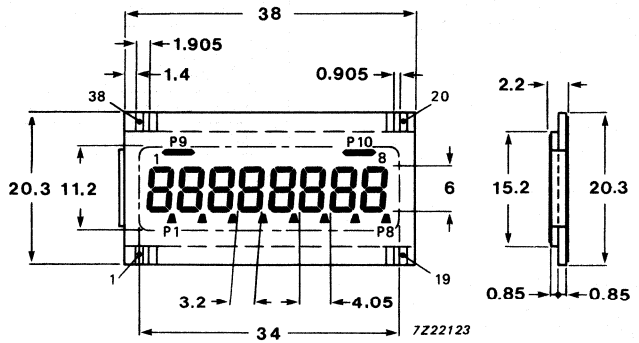


Fig.2 Display dimensions.

MULTIPLEX DUTY FACTOR 1:2

PIN NO.	COMMON 1	COMMON 2
1		comm 2
2	g1	e1
3	c1	d1
4	g2	e2
5	c2	d2
6	g3	e3
7	c3	d3
8	g4	e4
9	c4	d4
10	g5	e5
11	c5	d5
12	g6	e6
13	c6	d6
14	g7	e7
15	c7	d7
16	g8	e8
17	c8	d8
18		comm 2
19	comm 1	

PIN NO.	COMMON 1	COMMON 2
20	b8	P8
21	a8	f8
22	P10	
23	b7	P7
24	a7	f7
25	b6	P6
26	a6	f6
27	b5	P5
28	a5	f5
29	b4	P4
30	a4	f4
31	b3	P3
32	a3	f3
33	b2	P2
34	a2	f2
35	P9	
36	b1	P1
37	a1	f1
38	comm 1	

Preferred drivers: PCF2111, PCF8576, PCF8577

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range LTD211R-11, LTD211F-11 LTD211R-21, LTD211F-21	T_{stg}	 −25 to +70 °C −40 to +90 °C

CHARACTERISTICS

See family characteristics, multiplex drive 1:2

TYPE	FAMILY CHARACTERISTICS
LTD211R-11	TR1
LTD211F-11	TF1
LTD211R-21	TR2
LTD211F-21	TF2

Liquid crystal display LTD221

DEVICE DESCRIPTION

The LTD221R;F is a 3 ½-digit, 7-segment multi-function LCD. Typical applications include panel-meters, multimeters.

QUICK REFERENCE DATA

Viewing area dimensions	46.7 X 18.4 mm
Overall glass dimensions	50.8 X 30.4 mm
Thickness	2.5 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

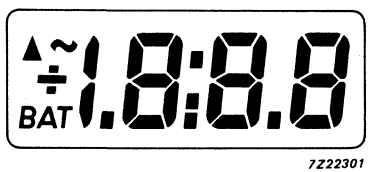


Fig.1 Universal display.

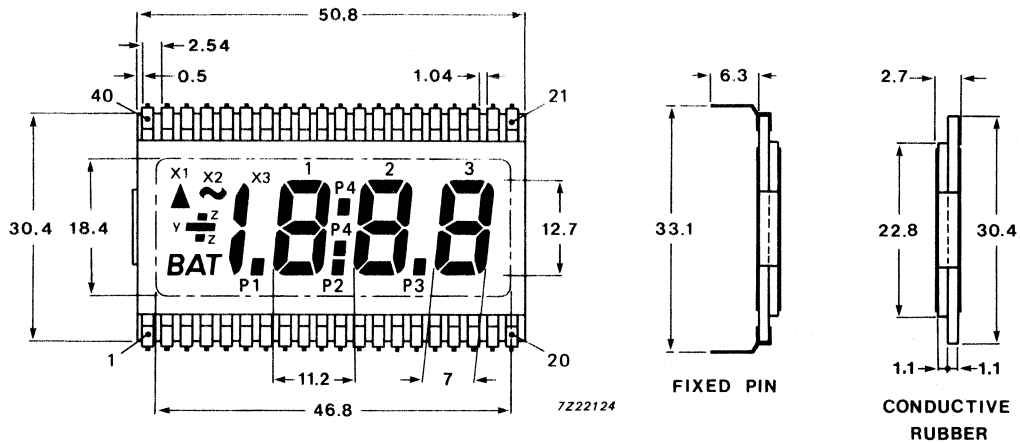
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD221R-11	reflective	for conductive rubber	−10 to 60 °C	commercial
LTD221R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTD221R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD221F-12	transflective	with fixed pin	−10 to 60 °C	commercial
LTD221F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112, PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	X3
4	
5	
6	
7	
8	p1
9	e1
10	d1
11	c1
12	p2
13	e2
14	d2
15	c2
16	p3
17	e3
18	d3
19	c3
20	b3

PIN NO.	SEGMENT
21	a3
22	f3
23	g3
24	b2
25	a2
26	f2
27	g2
28	p4
29	b1
30	a1
31	f1
32	g1
33	
34	
35	
36	
37	X2
38	X1
39	Z
40	BAT

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range LTD221R-12, LTD221F-12, LTD221R-11 LTD221R-22, LTD221F-22	T_{stg}	 −25 to +70 °C −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD221R-11	TR0
LTD221R-12	TR0
LTD221R-22	TR2
LTD221F-12	TF0
LTD221F-22	TF2

Liquid crystal display LTD222

DEVICE DESCRIPTION

The LTD222R: F is a 3 ½-digit, 7-segment multi-function LCD. Typical applications include panel-meters, multimeters.

QUICK REFERENCE DATA

Viewing area dimensions	46.7 X 18.4 mm
Overall glass dimensions	50.7 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

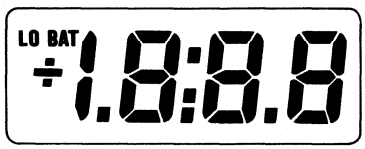


Fig.1 Multimeter display.

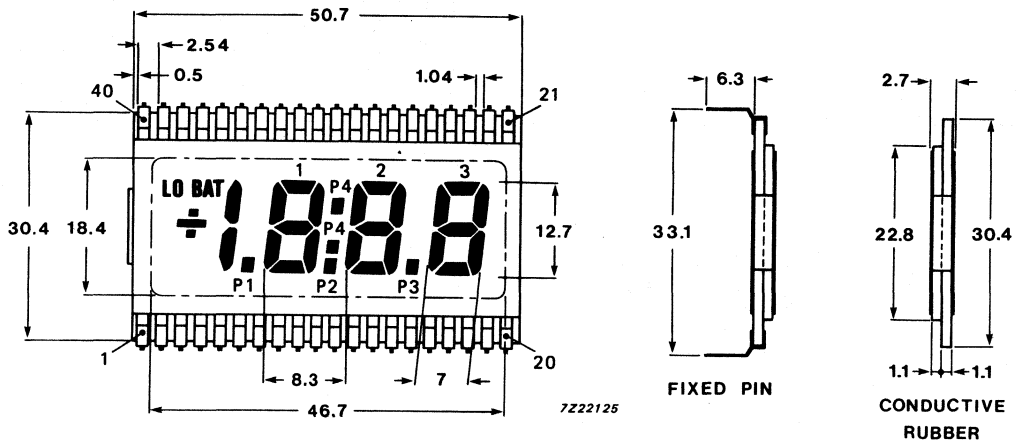
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD222R-11	reflective	for conductive rubber	−10 to 60 °C	commercial
LTD222R-12	reflective	with fixed pins	−10 to 60 °C	commercial
LTD222F-12	transflective	with fixed pin	−10 to 60 °C	commercial
LTD222R-21	reflective	for conductive rubber	−25 to 80 °C	extended
LTD222F-21	transflective	for conductive rubber	−25 to 80 °C	extended
LTD222R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD222F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112, PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	k
4	
5	
6	
7	
8	p1
9	e1
10	d1
11	c1
12	p2
13	e2
14	d2
15	c2
16	p3
17	e3
18	d3
19	c3
20	b3

PIN NO.	SEGMENT
21	a3
22	f3
23	g3
24	b2
25	a2
26	f2
27	g2
28	p4
29	b1
30	a1
31	f1
32	g1
33	
34	
35	
36	
37	
38	LOBAT
39	X
40	comm

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range LTD222R-11, LTD222R-12, LTD222F-12 LTD222R-21, LTD222F-21, LTD222R-22, LTD222F-22	T_{stg}	 −25 to +70 °C −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD222R-11	TR0
LTD222R-12	TR0
LTD222F-12	TF0
LTD222R-21	TR2
LTD222F-21	TF2
LTD222R-22	TR2
LTD222F-22	TF2

Liquid crystal display LTD224

DEVICE DESCRIPTION

The LTD224R-11 is a 3 ½-digit, 7-segment multi-function LCD with various additional indicators. It is intended for use in multimeters and panelmeters.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 X 17.8 mm
Overall glass dimensions	50.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

Fig.1 Multimeter display.

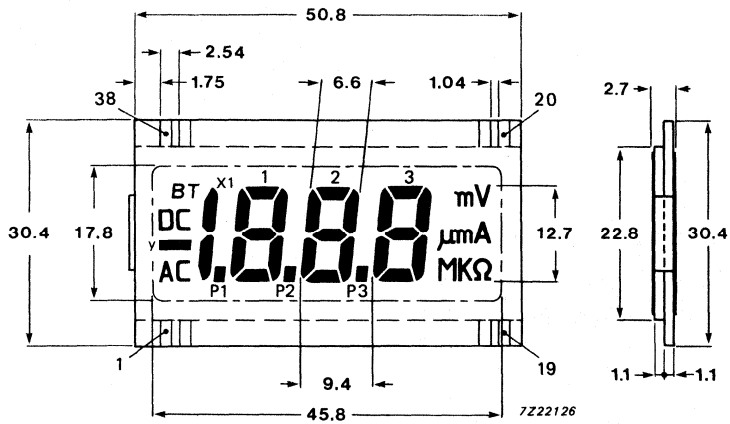
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD224R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF8576, PCF2111 (x2)

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	AC
2	Y
3	X1
4	p1
5	e1
6	d1
7	c1
8	p2
9	e2
10	d2
11	c2
12	p3
13	e3
14	d3
15	c3
16	M
17	K
18	Ω
19	A

PIN NO.	SEGMENT
20	V
21	m2
22	m1
23	µ
24	b3
25	a3
26	f3
27	g3
28	b2
29	a2
30	f2
31	g2
32	b1
33	a1
34	f1
35	g1
36	BT
37	DC
38	comm

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD224R-11	TR0

Liquid crystal display LTD225

DEVICE DESCRIPTION

The LTD225R-11 is a 3 ½-digit, 7-segment multi-function LCD. Typical applications include panel-meters, multimeters.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 X 17.8 mm
Overall glass dimensions	50.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

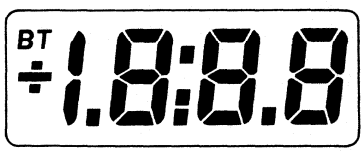


Fig.1 Multimeter display.

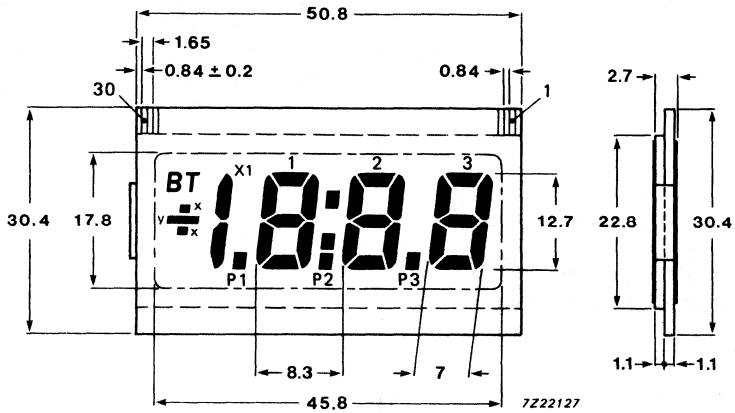
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD225R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred driver: PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	d3
2	c3
3	b3
4	a3
5	f3
6	g3
7	e3
8	P3
9	d2
10	c2
11	b2
12	a2
13	f2
14	g2
15	e2

PIN NO.	SEGMENT
16	P4
17	P2
18	d1
19	c1
20	b1
21	a1
22	f1
23	g1
24	e1
25	p1
26	x1
27	y
28	x
29	BT
30	comm

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD225R-11	TR0

Liquid crystal display LTD226

DEVICE DESCRIPTION

The LTD226R;F is a 4-digit, 7-segment multi-function LCD. Typical applications include 24 hr. clocks and industrial equipment.

QUICK REFERENCE DATA

Viewing area dimensions	46.7 X 18.4 mm
Overall glass dimensions	50.7 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

Fig.1 Universal display.

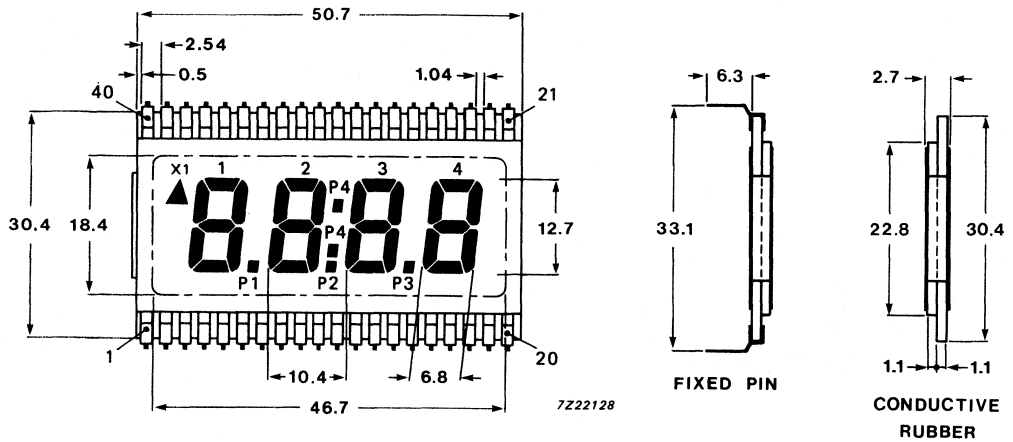
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD226R-11	reflective	for conductive rubber	−10 to 60 °C	commercial
LTD226R-12	reflective	with fixed pins	−10 to 60 °C	commercial
LTD226F-12	transflective	with fixed pins	−10 to 60 °C	commercial
LTD226R-21	reflective	for conductive rubber	−25 to 80 °C	extended
LTD226F-21	transflective	for conductive rubber	−25 to 80 °C	extended
LTD226R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD226F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112 (x2), PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	
3	
4	
5	e1
6	d1
7	c1
8	p1
9	e2
10	d2
11	c2
12	p2
13	e3
14	d3
15	c3
16	p3
17	e4
18	d4
19	c4
20	b4

PIN NO.	SEGMENT
21	a4
22	f4
23	g4
24	b3
25	a3
26	f3
27	g3
28	p4
29	b2
30	a2
31	f2
32	g2
33	
34	b1
35	a1
36	f1
37	g1
38	X1
39	
40	comm

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range		
LTD226R-11, LTD226R-12, LTD226F-12	T_{stg}	−25 to +70 °C
LTD226R-21, LTD226F-21, LTD226R-22, LTD226F-22		−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD226R-11	TR0
LTD226R-12	TR0
LTD226F-12	TF0
LTD226R-21	TR2
LTD226F-21	TF2
LTD226R-22	TR2
LTD226F-22	TF2

Liquid crystal display LTD227

DEVICE DESCRIPTION

The LTD227R; F is a 4 ½-digit, 7-segment multi-function LCD. Typical applications include panel-meters, multimeters.

QUICK REFERENCE DATA

Viewing area dimensions	46.8 x 18.8 mm
Overall glass dimensions	50.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	10.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

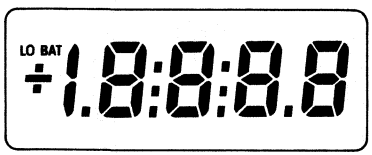


Fig.1 Multimeter display.

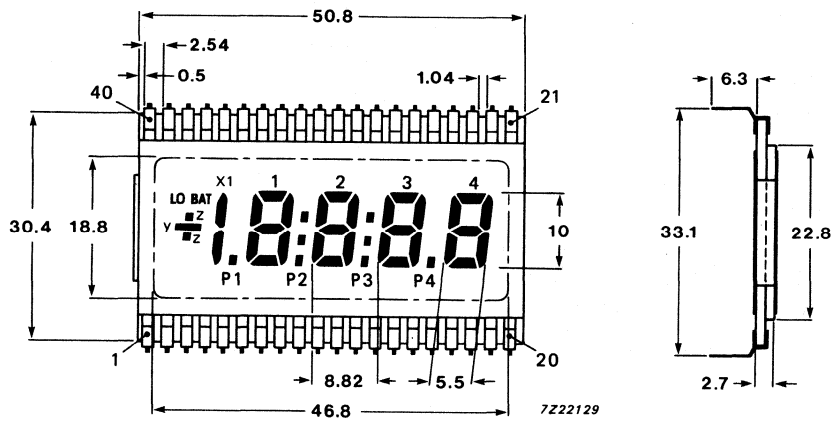
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD227R-12	reflective	with fixed pins	−10 to 60 °C	commercial
LTD227R-22	reflective	with fixed pins	−25 to 80 °C	extended
LTD227F-22	transflective	with fixed pins	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred driver: PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	X1
4	p1
5	e1
6	d1
7	c1
8	p2
9	e2
10	d2
11	c2
12	p3
13	e3
14	d3
15	c3
16	p4
17	e4
18	d4
19	c4
20	b4

PIN NO.	SEGMENT
21	a4
22	f4
23	g4
24	b3
25	a3
26	f3
27	g3
28	P6
29	b2
30	a2
31	f2
32	g2
33	P5
34	b1
35	a1
36	f1
37	g1
38	LOBAT
39	Z
40	nc

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature		
LTD227R-12	T_{stg}	−25 to +70 °C
LTD227R-22, LTD227F-22		−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD227R-12	TR0
LTD227R-22	TR2
LTD227F-22	TF2

Liquid crystal display LTD228

DEVICE DESCRIPTION

The LTD228R-12 is a 5-digit, 7-segment multi-function LCD. Typical applications include counters, instruments.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 × 17.8 mm
Overall glass dimensions	50.8 × 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	10.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

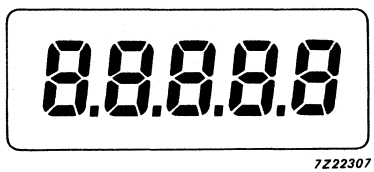


Fig.1 Universal LCD.

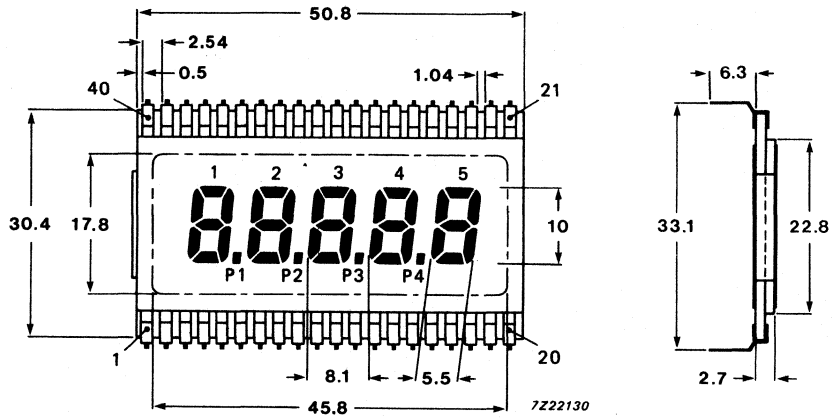
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD228R-12	reflective	with fixed pins	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF8576, PCF2112 (x2)

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	g1
3	e1
4	d1
5	c1
6	e2
7	d2
8	c2
9	e3
10	d3
11	c3
12	p3
13	e4
14	d4
15	c4
16	p4
17	e5
18	d5
19	c5
20	b5

PIN NO.	SEGMENT
21	a5
22	f5
23	g5
24	b4
25	a4
26	f4
27	g4
28	b3
29	a3
30	f3
31	g3
32	p2
33	b2
34	a2
35	f2
36	g2
37	p1
38	b1
39	a1
40	f1

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD228R-12	TR0

Liquid crystal display LTD229

DEVICE DESCRIPTION

The LTD229R;F is a 6-digit, 7-segment universal LCD. Typical applications include 24 hr. clocks with a seconds display, counters and instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 X 18.4 mm
Overall glass dimensions	69.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

Fig.1 Universal display.

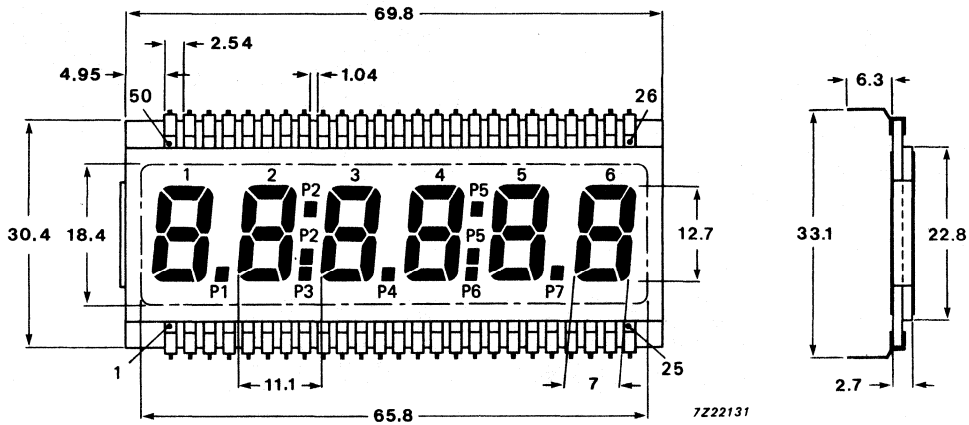
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD229R-12	reflective	with fixed pins	−10 to 60 °C	commercial
LTD229R-22	reflective	with fixed pins	−25 to 80 °C	extended
LTD229F-22	transflective	with fixed pins	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112 (x2), PCF8577 (x2)

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	e1
3	d1
4	c1
5	p1
6	e2
7	d2
8	c2
9	p3
10	e3
11	d3
12	c3
13	p4
14	e4
15	d4
16	c4
17	p6
18	e5
19	d5
20	c5
21	p7
22	e6
23	d6
24	c6
25	b6

PIN NO.	SEGMENT
26	a6
27	f6
28	g6
29	b5
30	a5
31	f5
32	g5
33	p5
34	b4
35	a4
36	f4
37	g4
38	b3
39	a3
40	f3
41	g3
42	p2
43	b2
44	a2
45	f2
46	g2
47	b1
48	a1
49	f1
50	g1

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range		
LTD229R-12	T_{stg}	−25 to +70 °C
LTD229R-22, LTD229F-22		−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD229R-12	TR0
LTD229R-22	TR2
LTD229F-22	TF2

Liquid crystal display LTD231

DEVICE DESCRIPTION

The LTD231R-11 is a 3 ½-digit, 7-segment multi-function LCD. Typical applications include multi-meters and panelmeters.

QUICK REFERENCE DATA

Viewing area dimensions	45.8 X 17.1 mm
Overall glass dimensions	50.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	10,2 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:3
Operating voltage V_{op}	3.2 to 3.45 V

DISPLAY MODE

Scale 1:1

Fig.1 Multimeter display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD231R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Unused segments to be controlled "off".

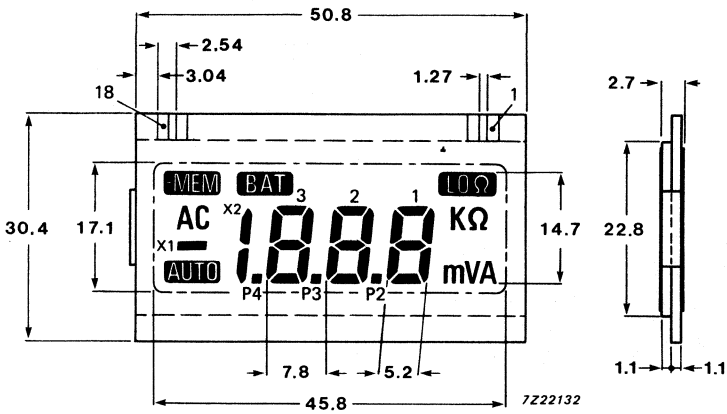


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3
1	comm 1		
2		comm 2	
3			comm 3
4		LO Ω	A
5		Ω	V
6		K	m
7	b1	c1	
8	a1	g1	d1
9	f1	e1	
10	b2	c2	P2
11	a2	g2	d2
12	f2	e2	
13	b3	c3	P3
14	a3	g3	d3
15	f3	e3	
16	b4	c4	P4
17	AC	X1	AUTO
18	BAT	-MEM	

Preferred drivers: TSC805, PCF8576

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, MUX 1:3

TYPE	FAMILY CHARACTERISTICS
LTD231R-11	TR1

Liquid crystal display LTD232

DEVICE DESCRIPTION

The LTD232R-11 is a 4 ½-digit, 7-segment multi-function LCD. Typical applications include multimeters and panelmeters.

QUICK REFERENCE DATA

Viewing area dimensions	44.8 X 16.8 mm
Overall glass dimensions	50.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	11.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:3
Operating voltage V_{op}	3.2 to 3.45 V

DISPLAY MODE

Scale 1:1

Fig.1 Multimeter display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD232R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Unused segments to be controlled "off".

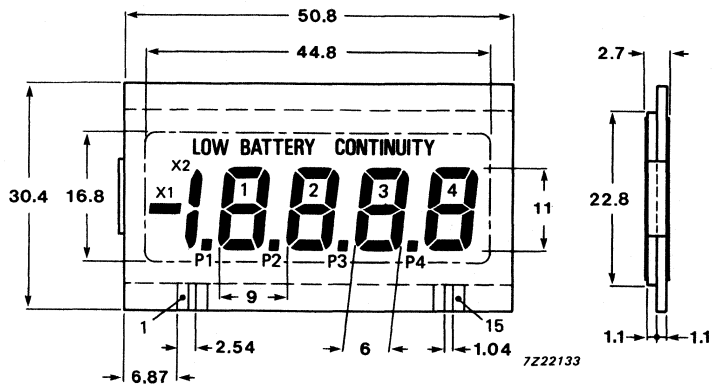


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3
1	f1	e1	P1
2	a1	g1	d1
3	b1	c1	X2
4	f2	e2	P2
5	a2	g2	d2
6	b2	c2	X1
7	f3	e3	P3
8	a3	g3	d3
9	b3	c3	LOW BATTERY
10	f4	e4	P4
11	a4	g4	d4
12	b4	c4	CONTINUITY
13	comm 1		
14		comm 2	
15			comm 3

Preferred driver: PCF8576

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, multiplex drive 1:3

TYPE	FAMILY CHARACTERISTICS
LTD232R-11	TR1

Liquid crystal display LTD233

DEVICE DESCRIPTION

The LTD233R-11 is a 16-digit, 7-segment display used for telephony.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 X 11.2 mm
Overall glass dimensions	69.8 X 20.3 mm
Thickness	2.2 ± 0.4 mm
Digit height	6.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:2
Operating voltage V_{op}	2.8 to 3.2 V

DISPLAY MODE

Scale 1:1

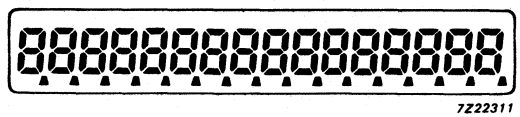


Fig.1 Telecom display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD233R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm

Unused segments to be controlled "off".

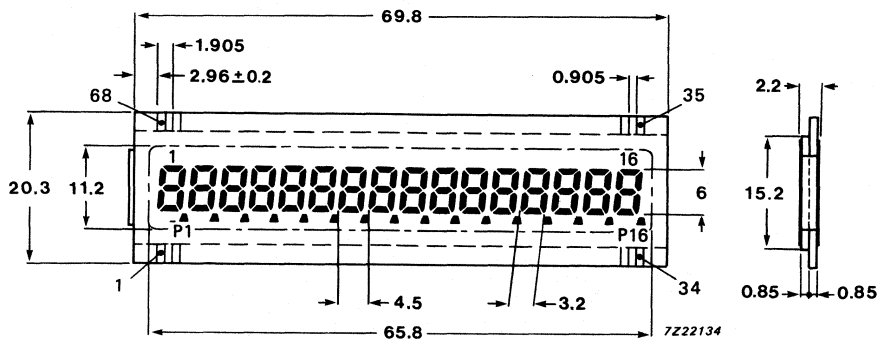


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2
1		comm 2
2	g1	e1
3	c1	d1
4	g2	e2
5	c2	d2
6	g3	e3
7	c3	d3
8	g4	e4
9	c4	d4
10	g5	e5
11	c5	d5
12	g6	e6
13	c6	d6
14	g7	e7
15	c7	d7
16	g8	e8
17	c8	d8
18	g9	e9
19	c9	d9
20	g10	e10
21	c10	d10
22	g11	e11
23	c11	d11
24	g12	e12
25	c12	d12
26	g13	e13
27	c13	d13
28	g14	e14
29	c14	d14
30	g15	e15
31	c15	d15
32	g16	e16
33	c16	d16
34		comm 2

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2
35	comm 1	
36	b16	P16
37	a16	f16
38	b15	P15
39	a15	f15
40	b14	P14
41	a14	f14
42	b13	P13
43	a13	f13
44	b12	P12
45	a12	f12
46	b11	P11
47	a11	f11
48	b10	P10
49	a10	f10
50	b9	P9
51	a9	f9
52	b8	P8
53	a8	f8
54	b7	P7
55	a7	f7
56	b6	P6
57	a6	f6
58	b5	P5
59	a5	f5
60	b4	P4
61	a4	f4
62	b3	P3
63	a3	f3
64	b2	P2
65	a2	f2
66	b1	P1
67	a1	f1
68	comm 1	

Preferred drivers: PCF2111 (x2); PCF8577 (x2)

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, multiplex drive 1:2

TYPE	FAMILY CHARACTERISTICS
LTD233R-11	TR1

Liquid crystal display LTD234

DEVICE DESCRIPTION

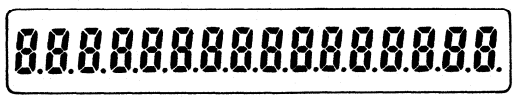
The LTD234R-21 is a 16-digit, 7-segment display used for telephony.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 X 11.2 mm
Overall glass dimensions	69.8 X 20.3 mm
Thickness	2.2 ± 0.4 mm
Digit height	6.0 mm
Preferred viewing direction	6 o'clock
Driving method	MUX 1:4
Operating voltage V_{op}	4.45 to 4.75 V

DISPLAY MODE

Scale 1:1



7Z22312

Fig.1 Universal display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD234R-21	reflective	for conductive rubber	−20/+70 °C	extended

MECHANICAL DATA

Dimensions in mm

Unused segments to be controlled "off".

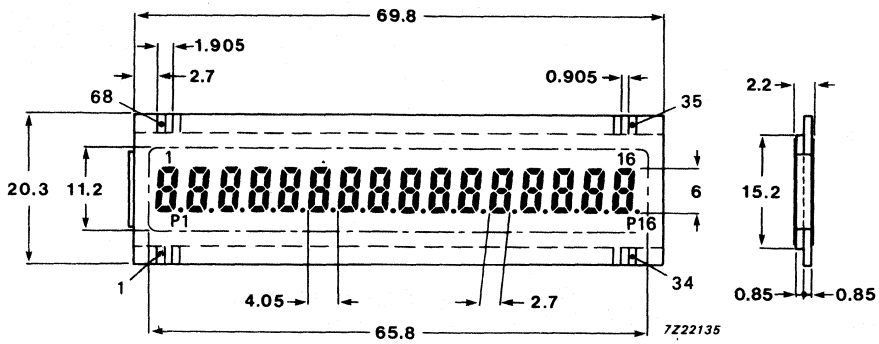


Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3	SEGMENTS ASSIGNED TO COMMON 4
1	comm 1			
2	comm 1			
3	e1	d1	g1	f1
4	e2	d2	g2	f2
5	NC			
6	e3	d3	g3	f3
7	NC			
8	e4	d4	g4	f4
9	NC			
10	e5	d5	g5	f5
11	NC			
12	e6	d6	g6	f6
13	NC			
14	e7	d7	g7	f7
15	NC		NC	
16	e8	d8	g8	f8
17	NC			
18	NC			
19	e9	d9	g9	f9
20	e10	d10	g10	f10
21	NC			
22	NC			
23	e11	d11	g11	f11
24	NC			
25	e12	d12	g12	f12
26	NC			
27	e13	d13	g13	f13
28	NC			
29	e14	d14	g14	f14
30	NC			
31	e15	d15	g15	f15
32	e16	d16	g16	f16
33		comm 2		
34		comm 2		

PIN DESCRIPTION (continued)

PIN NO.	SEGMENTS ASSIGNED TO COMMON 1	SEGMENTS ASSIGNED TO COMMON 2	SEGMENTS ASSIGNED TO COMMON 3	SEGMENTS ASSIGNED TO COMMON 4
35			comm 3	
36			comm 3	
37	c16	p16	b16	a16
38	c15	p15	b15	a15
39				
40				
41	c14	p14	b14	a14
42				
43	c13	p13	b13	a13
44				
45	c12	p12	b12	a12
46				
47	c11	p11	b11	a11
48				
49	c10	p10	b10	a10
50				
51	c9	p9	b9	a9
52				
53	c8	p8	b8	a8
54				
55	c7	p7	b7	a7
56				
57	c6	p6	b6	a6
58				
59	c5	p5	b5	a5
60				
61	c4	p4	b4	a4
62				
63	c3	p3	b3	a3
64				
65	c2	p2	b2	a2
66	c1	p1	b1	a1
67				comm 4
68				comm 4

Preferred driver: PCF8576

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−40 to +90 °C

CHARACTERISTICS

See family characteristics, multiplex drive 1:4

TYPE	FAMILY CHARACTERISTICS
LTD234R-21	TR2

Liquid crystal display LTD241

DEVICE DESCRIPTION

The LTD241R;F is a 3 ½-digit, 7-segment universal LCD with additional indicators. Typical applications include multimeters, panelmeters and industrial instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 X 26.0 mm
Overall glass dimensions	69.8 X 38.0 mm
Thickness	2.7 ± 0.4 mm
Digit height	17.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

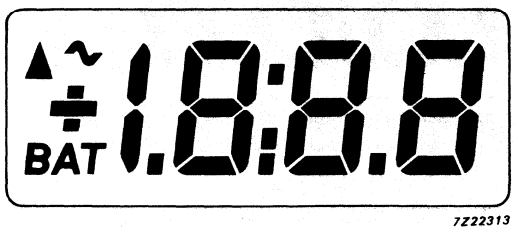


Fig.1 Multimeter display.

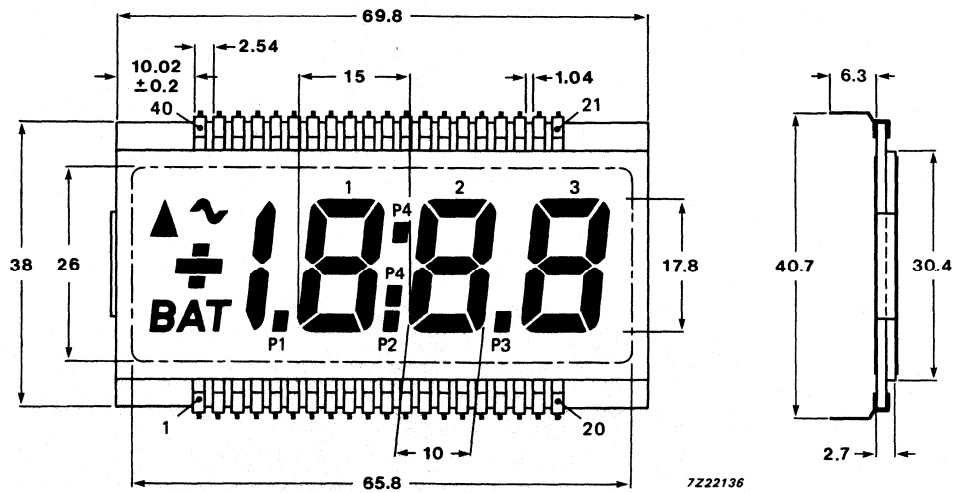
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD241R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTD241R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD241F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred driver: PCF2112

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	y
3	X3
4	
5	
6	
7	
8	p1
9	e1
10	d1
11	c1
12	p2
13	e2
14	d2
15	c2
16	p3
17	e3
18	d3
19	c3
20	b3

PIN NO.	SEGMENT
21	a3
22	f3
23	g3
24	b2
25	a2
26	f2
27	g2
28	p4
29	b1
30	a1
31	f1
32	g1
33	
34	
35	
36	
37	X2
38	X1
39	Z
40	BAT

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections — V_{max} — 15 V rms / 0.1 V DC

Storage temperature range

LTD241R-12	T_{stg}	−25 to +70 °C
LTD241R-22, LTD241F-22		−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD241R-12	TR0
LTD241R-22	TR2
LTD241F-22	TF2

Liquid crystal display LTD242

DEVICE DESCRIPTION

The LTD242R;F is a 4-digit, 7-segment universal LCD. Typical applications include 24 hr. clocks, counters and industrial equipment requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	65.8 X 26.0 mm
Overall glass dimensions	69.8 X 38.0 mm
Thickness	2.7 ± 0.4 mm
Digit height	17.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

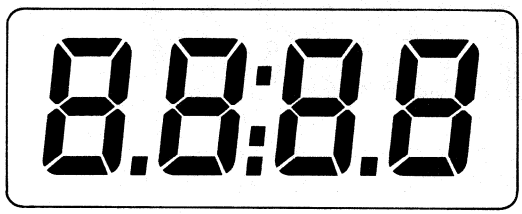


Fig.1 Universal display.

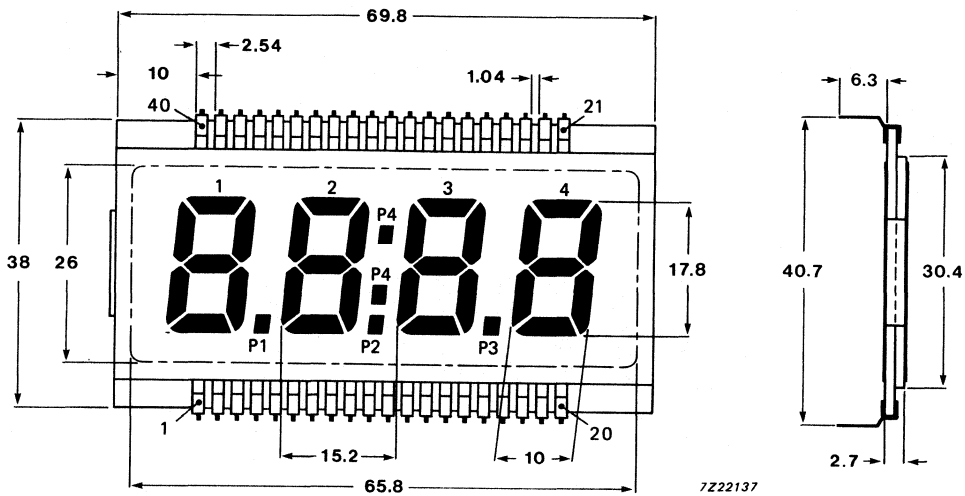
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD242R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTD242R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD242F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112, PCF8577

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	
3	
4	
5	e1
6	d1
7	c1
8	P1
9	e2
10	d2
11	c2
12	P2
13	e3
14	d3
15	c3
16	P3
17	e4
18	d4
19	c4
20	b4

PIN NO.	SEGMENT
21	a4
22	f4
23	g4
24	b3
25	a3
26	f3
27	g3
28	P4
29	b2
30	a2
31	f2
32	g2
33	
34	b1
35	a1
36	f1
37	g1
38	
39	
40	

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range LTD242R-12 LTD242R-22; LTD242F-22	T_{stg}	 −25 to +70 °C −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD242R-12	TR0
LTD242R-22	TR2
LTD242F-22	TF2

Liquid crystal display LTD261

DEVICE DESCRIPTION

The LTD261 is a 1-digit, 7-segment universal LCD. It can be combined to large clocks and displays requiring a large viewing distance.

QUICK REFERENCE DATA

Viewing area dimensions	71.2 × 89.0 mm
Overall glass dimensions	76.2 × 101.6 mm
Thickness	2.7 ± 0.4 mm
Digit height	76.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

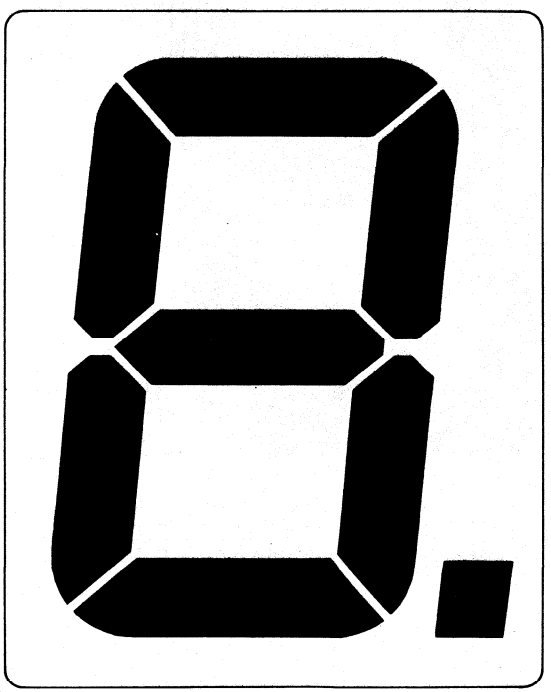
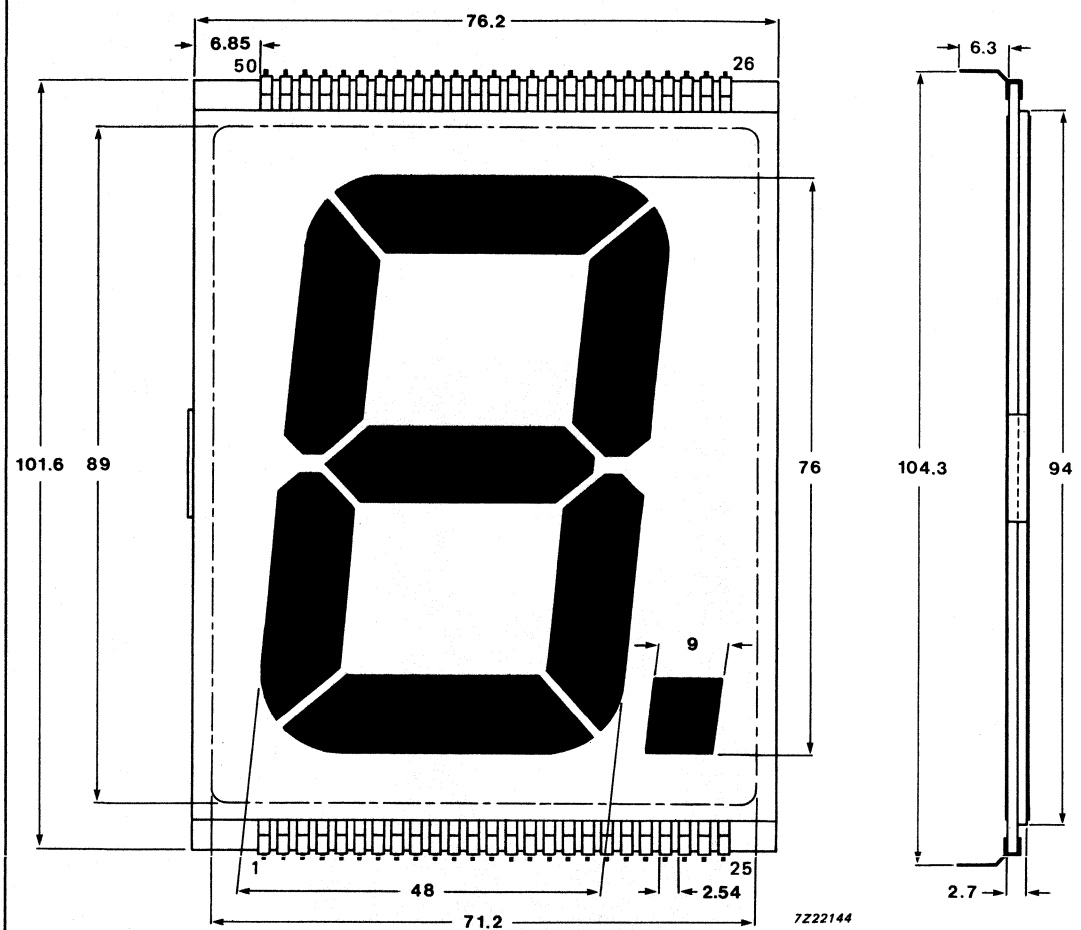


Fig.1 Universal display.

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112, PCF8577

Fig.2 Display dimensions.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD261R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTD261R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD261F-22	transflective	with fixed pin	−25 to 80 °C	extended

PIN DESCRIPTION

PIN NO.	SEGMENT
1-5	comm
6-10	e
11-15	d
16-20	c
21-25	P1

PIN NO.	SEGMENT
26-30	g
31-35	b
36-40	
41-45	a
46-50	f

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections — V_{max} — 15 V rms / 0.1 V DC

Storage temperature range — T_{stg}

LTD261R-12: −25 to +70 °C

LTD261R-22, LTD261F-22: −40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD261R-12	TR0
LTD261R-22	TR2
LTD261F-22	TF2

Liquid crystal display LTD262

DEVICE DESCRIPTION

The LTD262R;F is an 8-digit, 7-segment universal LCD. Typical applications include counters, timers and instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	89.8 X 18.4 mm
Overall glass dimensions	93.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	12.7 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

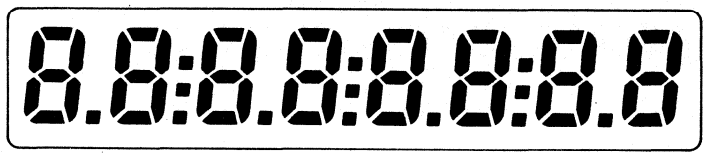


Fig.1 Universal display.

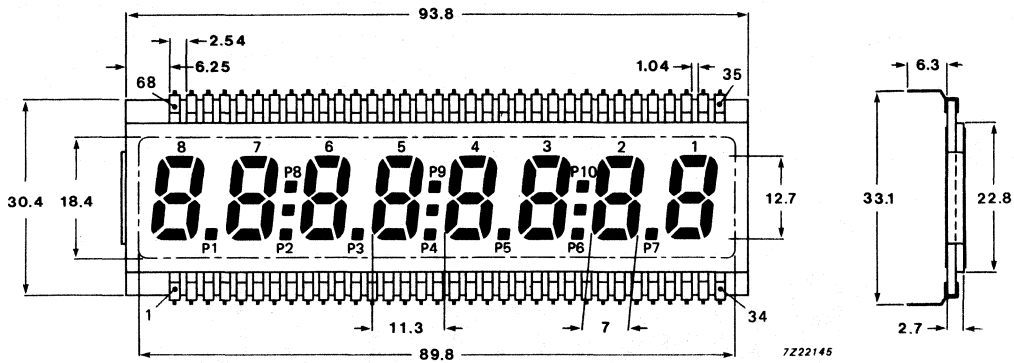
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD262R-12	reflective	with fixed pin	−10 to 60 °C	commercial
LTD262R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD262F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112 (x3), PCF8576 (x3)

Fig. 2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	e8
3	d8
4	c8
5	P1
6	e7
7	d7
8	c7
9	P2
10	
11	e6
12	d6
13	c6
14	P3
15	e5
16	d5
17	c5
18	P4
19	e4
20	d4
21	c4
22	P5
23	e3
24	d3
25	c3
26	P6
27	e2
28	d2
29	c2
30	P7
31	e1
32	d1
33	c1
34	b1

PIN NO.	SEGMENT
35	a1
36	f1
37	g1
38	b2
39	a2
40	f2
41	g2
42	P10
43	b3
44	a3
45	f3
46	g3
47	b4
48	a4
49	f4
50	g4
51	P9
52	b5
53	a5
54	f5
55	g5
56	b6
57	a6
58	f6
59	g6
60	P8
61	b7
62	a7
63	f7
64	g7
65	b8
66	a8
67	f8
68	g8

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range		
LTD262R-12	T_{stg}	−25 to +70 °C
LTD262R-22, LTD262F-22		−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD262R-12	TR0
LTD262R-22	TR2
LTD262F-22	TF2

Liquid crystal display LTD263

DEVICE DESCRIPTION

The LTD263 is a 6-digit, 7-segment universal LCD. Typical applications include 24 hr. clocks with a seconds display, counters and industrial instruments requiring a large display.

QUICK REFERENCE DATA

Viewing area dimensions	88.8 X 25.4 mm
Overall glass dimensions	93.8 X 38.0 mm
Thickness	2.7 ± 0.4 mm
Digit height	17.8 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

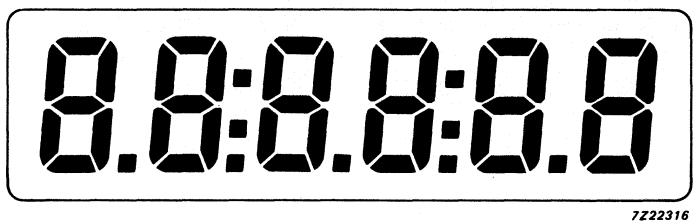


Fig.1 Universal display.

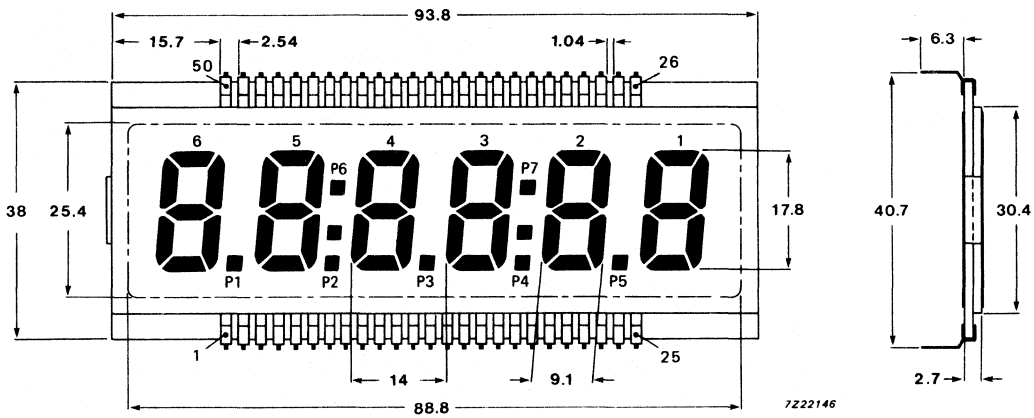
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD263R-12	reflective	with fixed pins	−10 to 60 °C	commercial
LTD263R-22	reflective	with fixed pins	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112 (x2), PCF8577 (x2)

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
	comm
2	e6
3	d6
4	c6
5	P1
6	e5
7	d5
8	c5
9	P2
10	e4
11	d4
12	c4
13	P3
14	e3
15	d3
16	c3
17	P4
18	e2
19	d2
20	c2
21	P5
22	e1
23	d1
24	c1
25	b1

PIN NO.	SEGMENT
26	a1
27	f1
28	g1
29	b2
30	a2
31	f2
32	g2
33	P7
34	b3
35	a3
36	f3
37	g3
38	b4
39	a4
40	f4
41	g4
42	P6
43	b5
44	a5
45	f5
46	g5
47	b6
48	a6
49	f6
50	g6

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range		
LTD263R-12	T_{stg}	−25 to +70 °C
LTD263R-22		−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD263R-12	TR0
LTD263R-22	TR2

Liquid crystal display LTD264

DEVICE DESCRIPTION

The LTD264R;F is an 5-digit, 7-segment point of sales display.

QUICK REFERENCE DATA

Viewing area dimensions	109.0 X 33.4 mm
Overall glass dimensions	114.0 X 46.0 mm
Thickness	2.7 ± 0.4 mm
Digit height	25.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

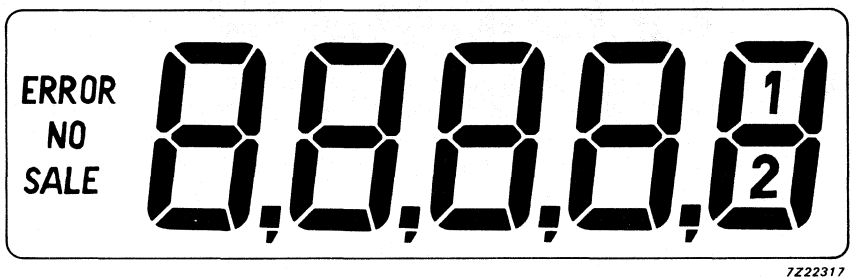


Fig.1 Till display.

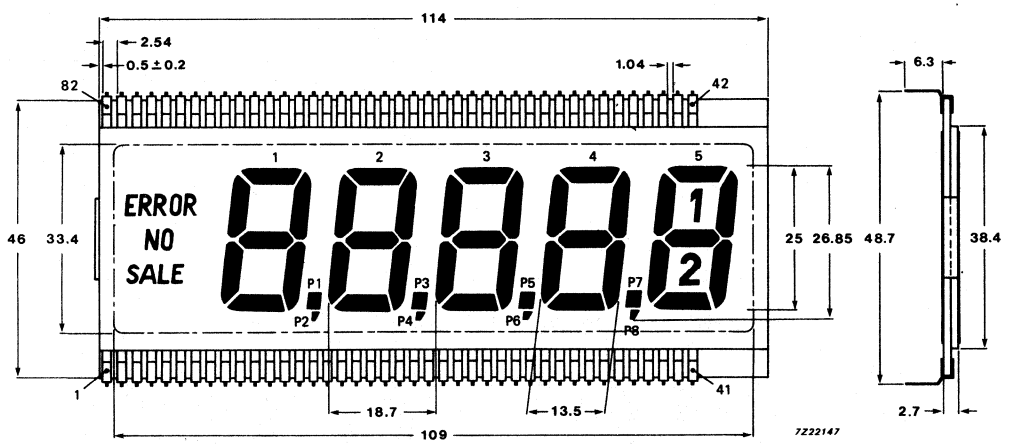
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD264R-22	reflective	with fixed pin	−25 to 80 °C	extended
LTD264F-22	transflective	with fixed pin	−25 to 80 °C	extended

MECHANICAL DATA

Dimensions in mm

Connect all unused segments to common.



Preferred drivers: PCF2112 (x2), PCF8577 (x2)

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT
1	comm
2	comm
3	comm
4	no sale
5	nc
6	nc
7	e1
8	d1
9	c1
10	nc
11	nc
12	nc
13	P1
14	P2
15	nc
16	nc
17	e2
18	d2
19	c2
20	nc
21	P3
22	P4
23	nc
24	e3
25	d3
26	c3
27	nc
28	P5
29	P6
30	nc
31	e4
32	d4
33	c4
34	nc
35	P7
36	P8
37	nc
38	e5
39	d5
40	2
41	c5

PIN NO.	SEGMENT
42	b5
43	1
44	a5
45	f5
46	g5
47	b4
48	a4
49	f4
50	g4
51	nc
52	nc
53	nc
54	b3
55	a3
56	f3
57	g3
58	nc
59	nc
60	nc
61	b2
62	a2
63	f2
64	g2
65	nc
66	nc
67	nc
68	nc
69	nc
70	b1
71	a1
72	f1
73	g1
74	nc
75	nc
76	nc
77	nc
78	nc
79	error
80	nc
81	nc
82	nc

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−40 to +90 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD264R-22	TR2
LTD264F-22	TF2

Liquid crystal display LTD321

DEVICE DESCRIPTION

The LTD321R-12 is a bargraph display. Typical applications include panelmeters and general purpose bargraph displays.

QUICK REFERENCE DATA

Viewing area dimensions	64.8 X 17.8 mm
Overall glass dimensions	69.8 X 30.4 mm
Thickness	2.7 ± 0.4 mm
Digit height	5.0 mm
Preferred viewing direction	6 o'clock
Driving method	direct drive
Operating voltage V_{op}	3 to 6 V

DISPLAY MODE

Scale 1:1

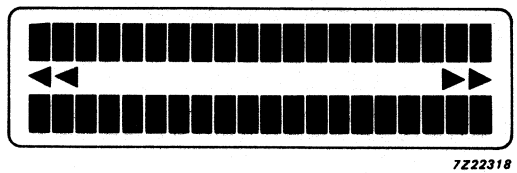


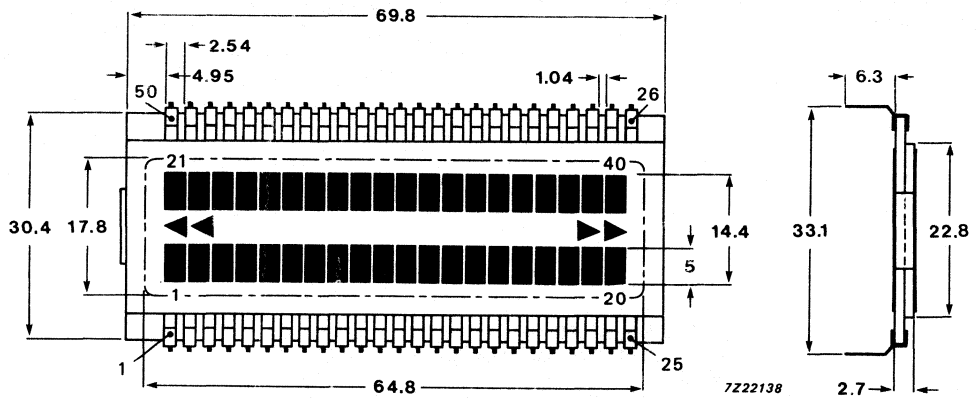
Fig.1 Universal bargraph display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD321R-12	reflective	with fixed pin	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm



Unused segments to be controlled "off".

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1	PIN NO.	SEGMENT ASSIGNED TO COMMON 2
1	comm 1	26	
2	1	27	
3	2	28	X4
4	3	29	X3
5	4	30	40
6	5	31	39
7	6	32	38
8	7	33	37
9	8	34	36
10	9	35	35
11	10	36	34
12	11	37	33
13	12	38	32
14	13	39	31
15	14	40	30
16	15	41	29
17	16	42	28
18	17	43	27
19	18	44	26
20	19	45	25
21	20	46	24
22	X1	47	23
23	X2	48	22
24		49	21
25		50	comm 2

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, direct drive

TYPE	FAMILY CHARACTERISTICS
LTD321R-12	TR0

Liquid crystal display LTD351

DEVICE DESCRIPTION

The LTD351R-12 is a bargraph display. Typical applications include panelmeters and general purpose bargraph displays.

QUICK REFERENCE DATA

Viewing area dimensions	16.0 X 109.0 mm
Overall glass dimensions	26.0 X 114.0 mm
Thickness	2.7 ± 0.4 mm
Digit height	5.0 mm
Preferred viewing direction	3 o'clock
Driving method	MUX 1:2
Operating voltage V_{op}	3.0 to 3.2 V

DISPLAY MODE

Scale 1:1

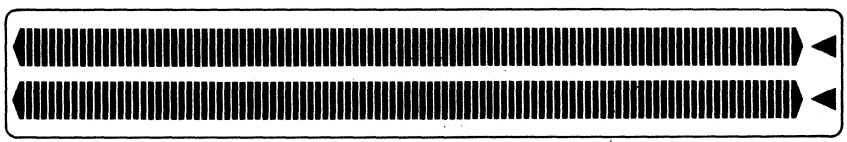


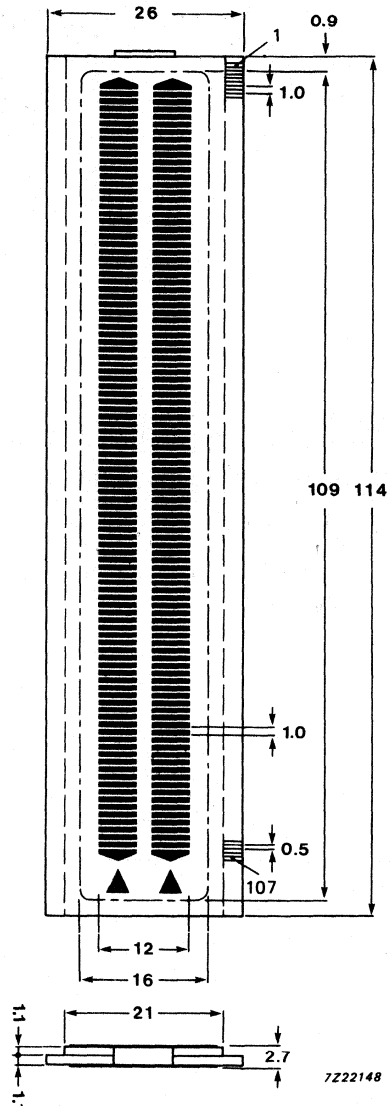
Fig.1 Universal bargraph display.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	CONNECTION METHOD	AMBIENT OPERATING TEMPERATURE RANGE	QUALITY GRADE
LTD351R-11	reflective	for conductive rubber	−10 to 60 °C	commercial

MECHANICAL DATA

Dimensions in mm



Unused segments to be controlled "off".

Fig.2 Display dimensions.

PIN DESCRIPTION

PIN NO.	SEGMENT ASSIGNED TO COMMON 1
1	comm 1
2	
3	
4	x1
.	.
.	.
.	.
107	x104

PIN NO.	SEGMENT ASSIGNED TO COMMON 2
1	
2	comm 2
3	comm 2
4	y1
.	.
.	.
.	.
107	y104

RATINGS

Limiting ratings in accordance with Absolute Maximum System (IEC 134)

Maximum voltage between any two connections	V_{max}	15 V rms 0.1 V DC
Storage temperature range	T_{stg}	−25 to +70 °C

CHARACTERISTICS

See family characteristics, MUX 1:2

TYPE	FAMILY CHARACTERISTICS
LTD351R-11	TR1

Liquid crystal display LXL401

DEVICE DESCRIPTION

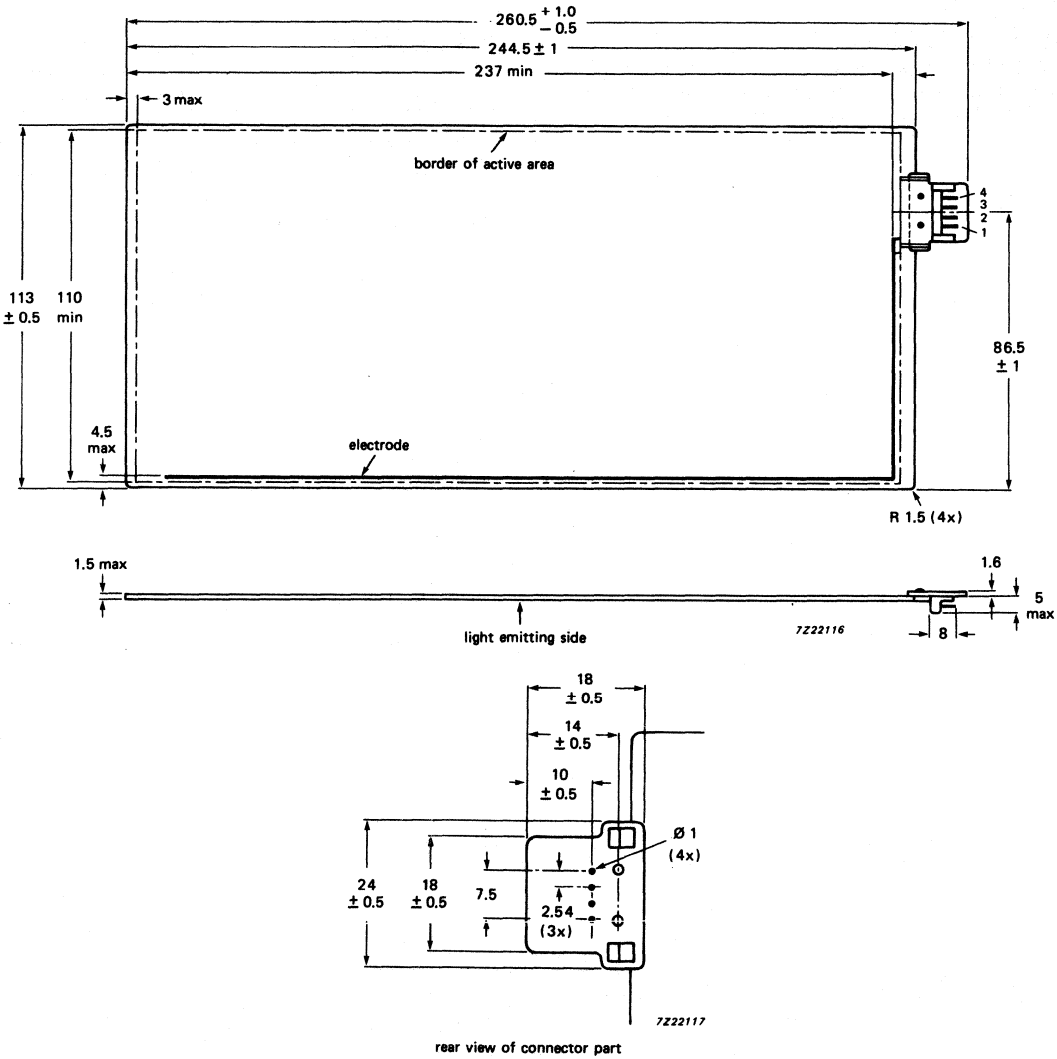
The LXL401-W is an electroluminescent backlight panel which has to be used in the LTG401F-10 LCD module. The emitted colour is white.

QUICK REFERENCE DATA

Outline dimensions	244.5 X 113 mm (excl. connector)
Supply voltage	100 V rms
Supply frequency	400 Hz
Colour	white

MECHANICAL DATA

Dimensions in mm



Pin connections

The device is connected between pins 1 and 4. Pins 2 and 3 are not connected.

A mating connector is the HNC2-2-5S-4.

Fig.1 Electro-luminescent backlight panel.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

Supply voltage peak to peak, f = 400 Hz, t = 60 s max	V_S	max.	150	V rms
Frequency V_S = 100 V rms, t = 60 s max	F	max.	900	Hz
Isolation voltage pin to film, t = 60 s max	V_{IS}	max.	1000	V rms
Storage temperature range	T_{stg}	−25 to +60		°C
Ambient operating temperature range	T_{amb}	0 to +50		°C

CHARACTERISTICS

T_{amb} = 25 °C, V_S = 100 Vrms, F = 400 Hz, in dark room unless otherwise specified

Luminence	L	typ.	50	nt
Supply current	I_S	typ.	42	mA
Capacitance	X	typ.	100	nF
Chromaticity (colour = white)	X	typ.	0.18	
	Y	typ.	0.4	

LCD module data

Liquid crystal display LTG201

MODULE DESCRIPTION

The LTG201R-10 is a 240 X 64 full dot LCD module. The module incorporates column and row driver LSI ICs and a temperature compensation circuit mounted on a single PC-board. The module is capable of displaying graphics, figures and symbols if connected to a microprocessor or specially designed LSI IC.
Using 5 X 7 dot character format the module can display up to 8 lines of 40 characters.

QUICK REFERENCE DATA

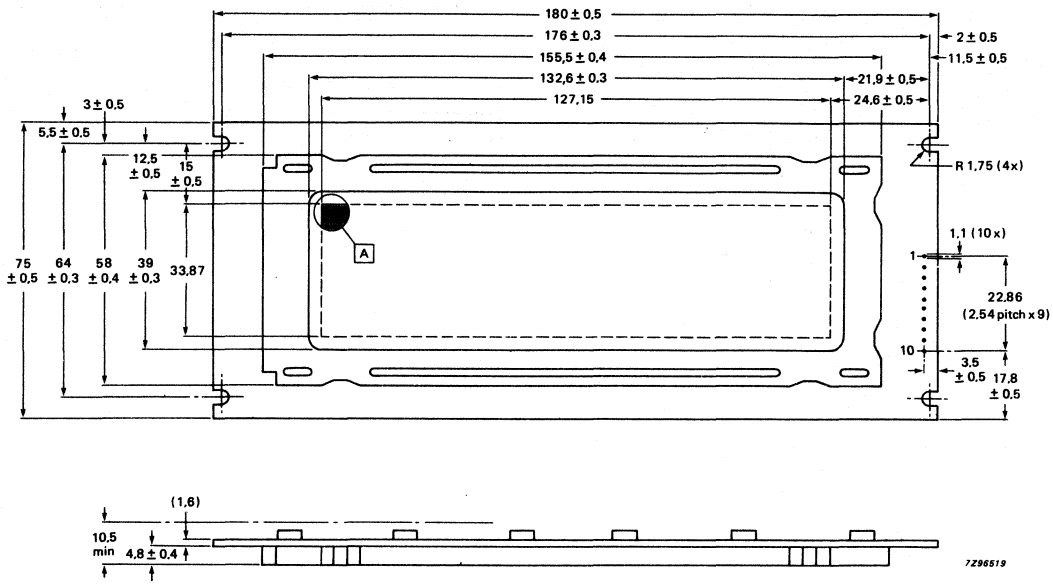
Outline dimensions	180 X 75 X 10.5 mm
Viewing area	132.6 X 39.0 mm
Dot size (spacing 0.05 mm)	0.48 X 0.48 mm
Mass	≈ 120 g
Drive method	MUX 1:64
Supply voltage	+5; −11 V
Power consumption	30 mW
Temperature compensation circuit	built in
Data interface	one bit serial
Controller	external
Illumination mode	reflective

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	TO BE USED WITH EL BACKLIGHT
LTG201R-10	reflective	–

MECHANICAL DATA

Dimensions in mm



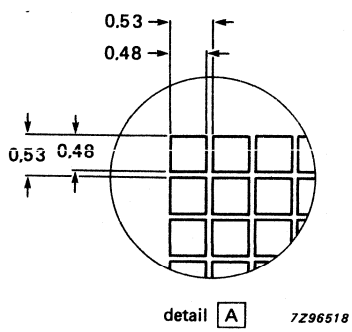


Fig.1 Module dimensions.

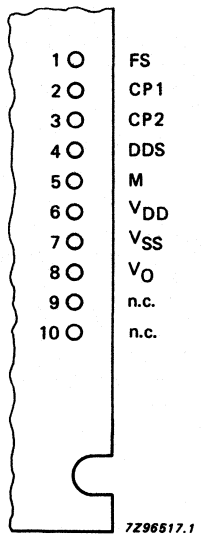


Fig.2 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND DESCRIPTION
1	FS	frame synch. input
2	CP1*	data clock pulse (latch)
3	CP2**	data clock pulse (shift)
4	DDS	display data signal
5	M	signal to convert the LCD drive waveform into AC
6	V_{DD}	power supply (logic)
7	V_{SS}	ground
8	V_O	contrast adjustment voltage
9	n.c.	not connected
10	n.c.	not connected

* CP1: latch column drivers; shift row drivers

** CP2: shift clock pulse for column data

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134); T_{amb} = 25 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	$V_{DD}-V_{SS}$	0	–	6.0	V
Supply voltage (LCD driver)	$V_{DD}-V_O$	0	–	18.0	V
Input voltage	V_I	0	–	V_{DD}	V
Storage temperature	T_{stg}	−25	–	+60	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltage values refer to V_{SS}; unless otherwise stated

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	−12.0	−11.0	–	V
LOW level input voltage	V_{IL}	0.0	–	0.2 V_{DD}	V
HIGH level input voltage	V_{IH}	0.8 V_{DD}	–	V_{DD}	V
LOW level input leakage current	I_{IL}	−10.0	–	–	μA
HIGH level input leakage current	I_{IH}	–	–	10	μA
Supply current (logic) see note	I_{DD}	–	6.0	12.0	mA
Supply current (LCD driver) see note	I_O	–	1.0	2.0	mA
Power dissipation see note	P_d	–	41.0	82.0	mW
Input capacitance					
pin 1	C_I	–	50.0	–	pF
pins 2 and 5	C_I	–	200.0	–	pF
pin 3	C_I	–	250.0	–	pF
pin 4	C_I	–	100.0	–	pF

Note: V_{DD} = 5 V; V_O = −11 V; f = 80 Hz.

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
HIGH level clock pulse width (CP1)	t_{WH1}	400	–	–	ns
HIGH level clock pulse width (CP2)	t_{WH2}	125	–	–	ns
LOW level clock pulse width (CP2)	t_{WL2}	125	–	–	ns
Maximum clock frequency	f_{cp2}	–	–	3.3	MHz
Data set-up time	t_{dsu2}	100	–	–	ns
Data hold time	t_{dh2}	100	–	–	ns
Clock rise time	t_{r2}, t_{rM}	–	–	50	ns
Clock fall time	t_{f2}	–	–	50	ns
Data set-up time	t_{dsu1}	100	–	–	ns
Data hold time	t_{dh1}	800	–	–	ns
Clock rise time	t_{r1}	–	–	1	μs
Clock fall time	t_{f1}	–	–	1	μs
Clock allowance time from CP1 ↓ to CP2	t_{HL12}	20	–	–	ns
Clock allowance time from CP2 ↓ to CP1	t_{HL21}	250	–	–	ns
Set-up time to CP1 ↑ against CP2 ↑	t_{LH12}	175	–	–	ns
Set-up time to CP2 ↑ against CP1 ↑	t_{LH21}	20	–	–	ns
Clock allowance time to M against CP1 ↓	t_M	100	–	–	ns

DRIVING METHOD

The circuit configuration is shown in Fig.5.

Input data and control signals

Input data and clock pulse are entered at the input data pin (pin 4) and the CP2 (pin 3) respectively; starting at the top left of display. The data input is implemented in the form of 1-bit serial data (HIGH level-turn on, LOW level-turn off).

On the falling edge of CP2 clock the input data is sequentially transferred via the shift register in the signal electrode driver.

After 1 row of data (240 dots) has been entered it is latched in the form of parallel data corresponding to 240 lines of signal electrodes. The data is dispatched to the signal electrodes after is has been latched. The data displayed will be according to the combination of voltages applied to the scan and signal electrodes of the LCD. The scan sequence is started by signal FS clocking a logic 1 on the falling edge of CP1. As the first row of the display is scanning the second row information is clocked in.

When the second rows 240 dots of data have been entered and latched on the falling edge of the CP1 clock, the display starts to scan the second row.

The display input is repeated up to the 64th row to complete the whole area of the display, then the data input proceeds to the next display face.

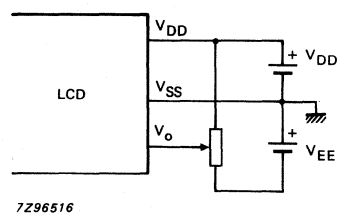


Fig. 3 Contrast adjustment circuit.

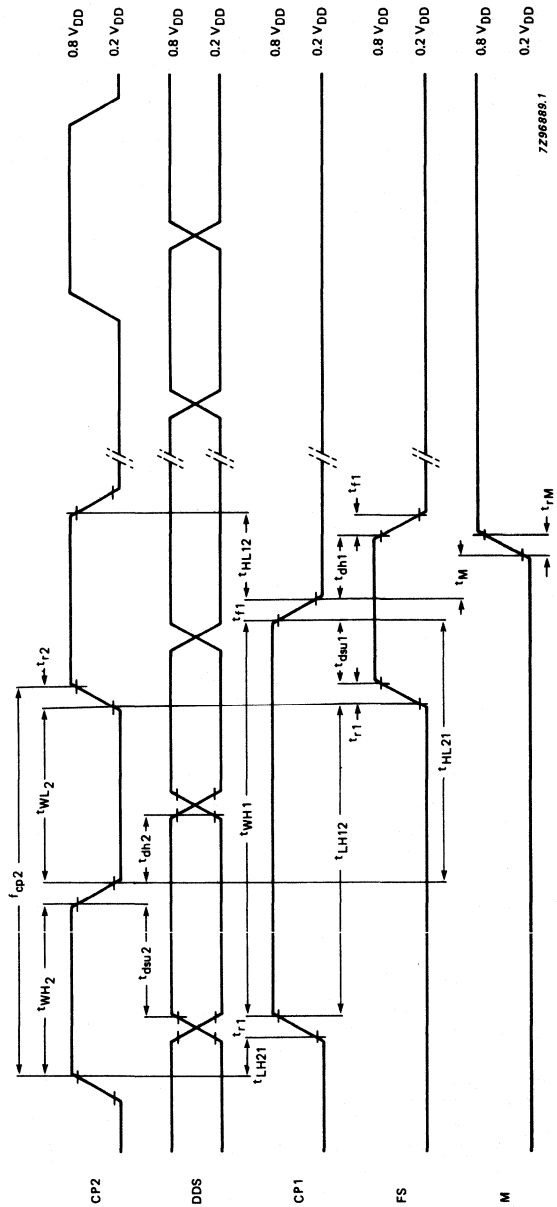


Fig. 4a Timing waveforms.

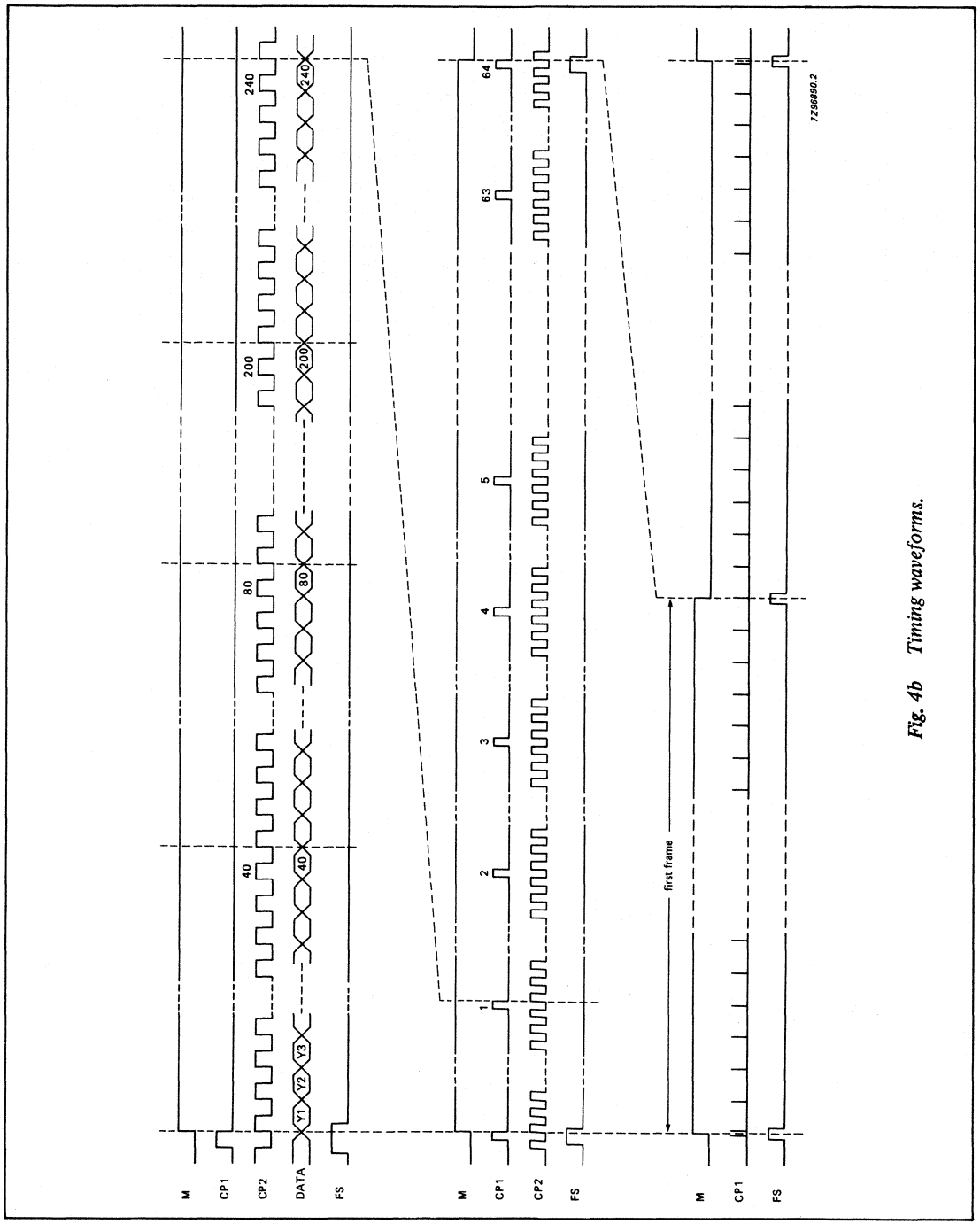


Fig. 4b Timing waveforms.

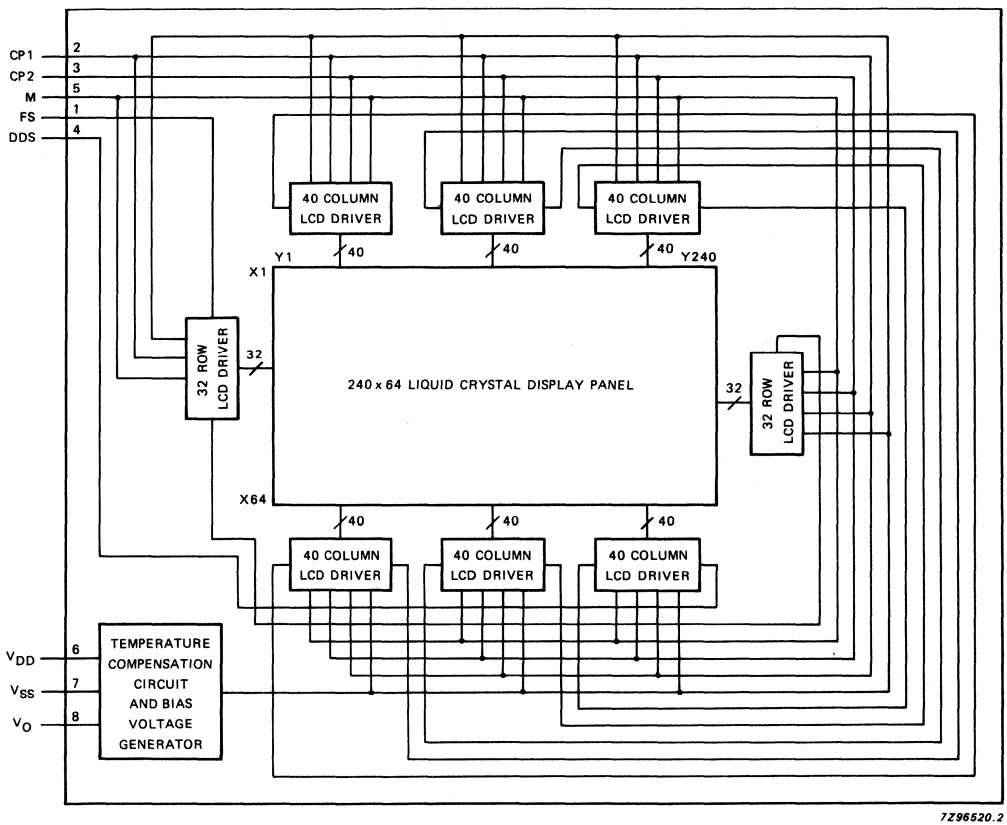


Fig.5 Module circuit diagram.

Preferred controllers: LR3691; MSM6240; HD61830.

Liquid crystal display LTG401

MODULE DESCRIPTION

The LTG401F-10 is a 640 X 200 dot, graphic LCD module. It should be used with an electro-luminescent (EL) backlight (LXL401-W) and offers a wide graphic display area incorporating up to 25 lines of 106. 5 X 7 dot characters.

QUICK REFERENCE DATA

Outline dimensions	256 X 125 X 18 mm
Viewing area	232 X 106 mm
Dot size (spacing 0.04 mm)	0.31 X 0.45 mm
Mass	≈ 470 g
Drive method	MUX 1:100
Supply voltage	+5; −18 V
Data interface	parallel 2 X 4 bits
Controller	external
Illumination mode	transflective
Illumination (EL backlight)	LXL401-W

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	TO BE USED WITH EL BACKLIGHT
LTG401F-10	transflective	LXL401-W

MECHANICAL DATA

Dimensions in mm

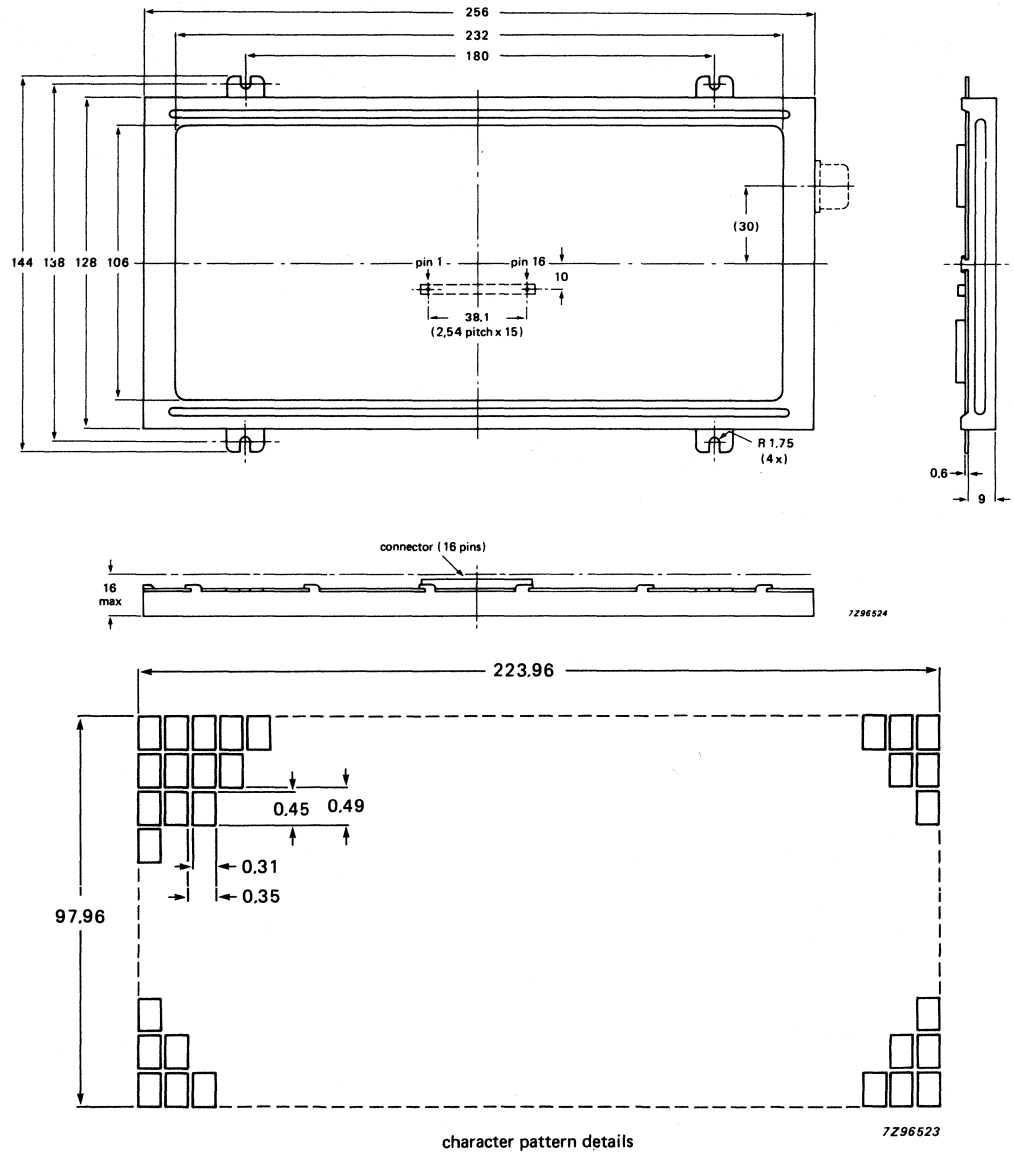


Fig.1 Module dimensions.

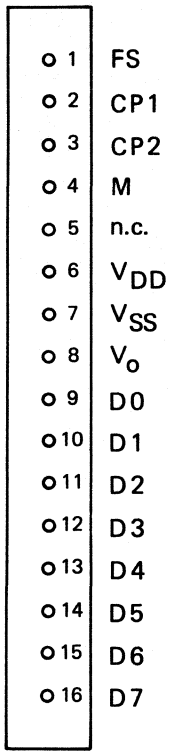


Fig.2 Pin configuration.

Note: Pins D0 to D3 are for the upper half of the display and pins D4 to D7 are for the lower half.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	FS	frame synch input
2	CP1	clock pulse (latch)
3	CP2	clock pulse (data)
4	M	signal to convert the LCD drive waveform into AC
5	n.c.	not connected
6	V_{DD}	power supply (logic)
7	V_{SS}	ground
8	V_O	contrast adjustment voltage
9	D0	display data signal
10	D1	display data signal
11	D2	display data signal
12	D3	display data signal
13	D4	display data signal
14	D5	display data signal
15	D6	display data signal
16	D7	display data signal

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	$V_{DD}-V_{SS}$	0	–	6.0	V
Supply voltage (LCD driver)	$V_{DD}-V_O$	0	–	28.0	V
Input voltage	V_I	0	–	V_{DD}	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltages refer to V_{SS}; unless otherwise stated

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	−23.0	–	−14.0	V
LOW level input voltage	V_{IL}	0.0	–	0.2 V_{DD}	V
HIGH level input voltage	V_{IH}	0.8 V_{DD}	–	V_{DD}	V
LOW level input leakage current	I_{IL}	−20.0	–	20	μA
Supply current (logic)	I_{DD}	–	25.0	30.0	mA
Supply current (LCD driver) (see note)	I_O	–	20.0	25.0	mA
Power dissipation	P_d	–	485	–	mW
Input capacitance					
pin 1	C_I	–	50.0	–	pF
pins 2 and 4	C_I	–	200.0	–	pF
pin 3	C_I	–	250.0	–	pF
pins 9 to 16	C_I	–	100.0	–	pF

Note: V_O = −18 V
V_{DD} = 5 V
frame frequency = 80 Hz
HIGH frequency display pattern.

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
HIGH level clock pulse width (CP2)	t_{WH2}	230	–	–	ns
LOW level clock pulse width (CP2)	t_{WL2}	230	–	–	ns
HIGH level clock pulse width (CP1)	t_{WH1}	130	–	–	ns
Data set-up time	t_{dsu1}	100	–	–	ns
Data hold time	t_{dh1}	100	–	–	ns
Clock rise time	t_r	–	–	30	ns
Clock fall time	t_f	–	–	30	ns
Data set-up time	t_{dsu2}	70	–	–	ns
Data hold time	t_{dh2}	50	–	–	ns
Clock allowance time	t_{CP12}	20	–	–	ns
Clock allowance time	t_{CP21u}	20	–	–	ns
Clock allowance time	t_{CP21d}	20	–	–	ns

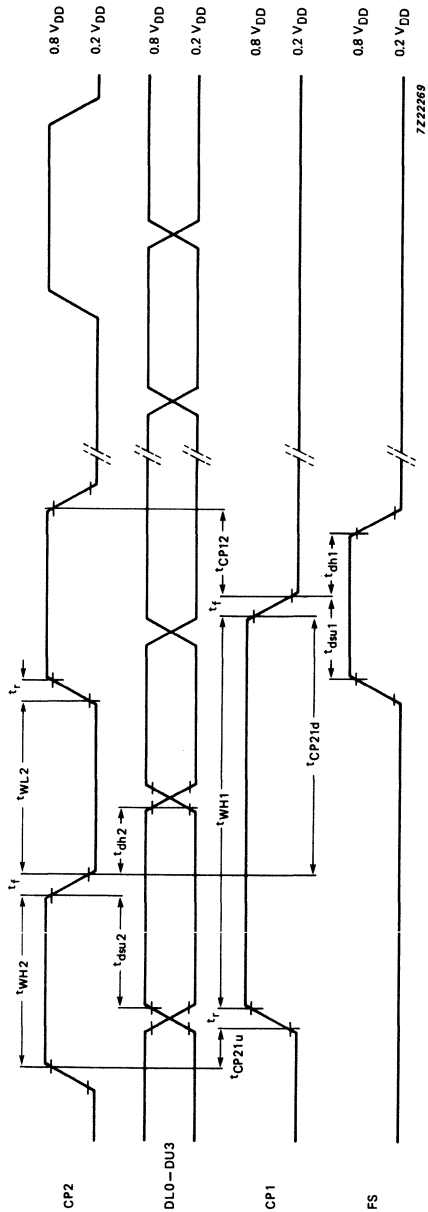


Fig.3 Timing waveforms.

DRIVING METHOD

The circuit configuration is shown in Fig.5.

Display face configuration

To enable a higher contrast the display face is separated into two display segments (upper and lower segments). This separation allows a reduction in the multiplex ratio so that each display segment (640 X 100 dots) is driven at a multiplex ratio of 1:100.

Input data and control signals

Display data is externally divided into data for each row (640 dots) and is implemented in the form of 4-bit parallel data.

On the falling edge of CP2 the input data is sequentially transferred into the shift register in the column drivers. On the falling edge of CP1 the data is latched and displayed.

The scan sequence is started by clocking signal FS in on the HIGH to LOW transition of clock pulse CP1 after which the first row is scanning and the second row information is clocked in by CP2.
When all the data of row 2 has been entered and latched on the falling edge of the CP1, the display proceeds to scanning the second row.
The data input continues until the whole area of the display is filled and then proceeds to the next display face.

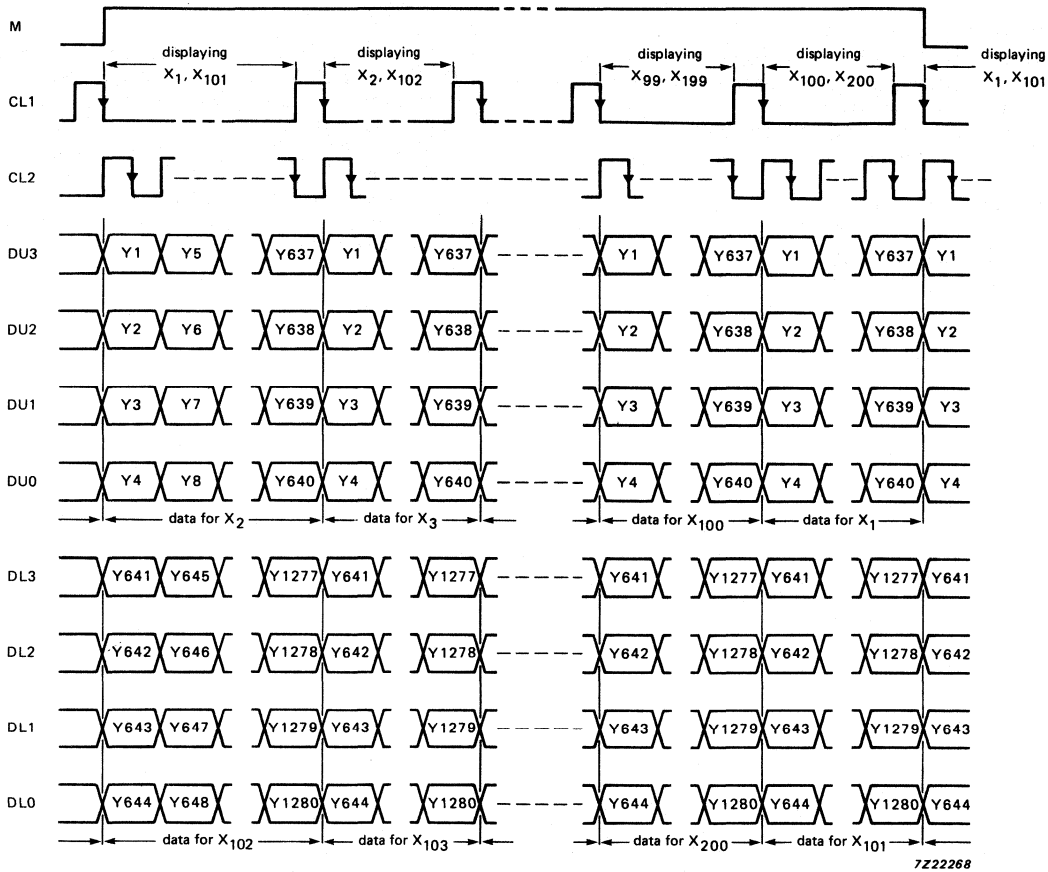


Fig.4 Data timing chart.

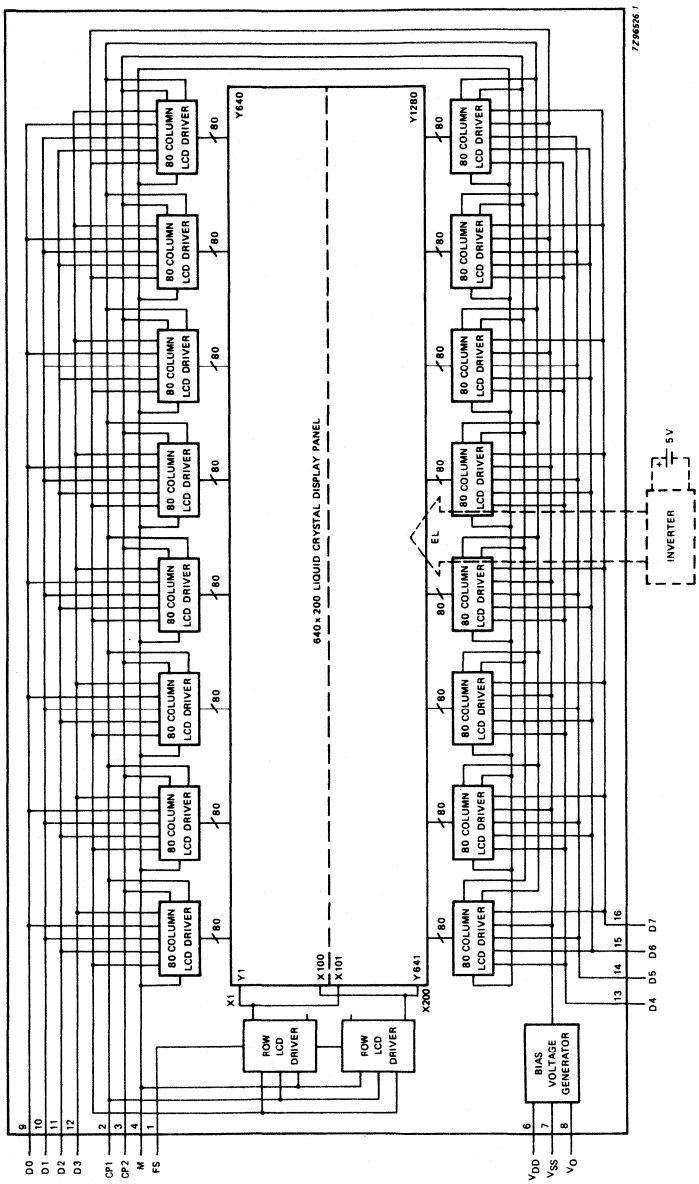


Fig.5 Module circuit diagram.

Liquid crystal display LTM233

MODULE DESCRIPTION

The LTM233R-10 is a 16-digit, 1-line, multiplex drive LCD module with a multiplex drive ratio of 1:2. The module is driven by 2 PCF2111 LCD drivers which are contained within the module housing. An external microcomputer can be programmed to supply display data of 16 numeric characters with some alphabetic characters possible.

QUICK REFERENCE DATA

Outline dimensions	92.5 X 25.0 X 10.5 mm
Viewing area	65.8 X 11.2 mm
Character size	3.2 X 6.0 mm
Mass	≈ 21.0 g
Drive method	MUX 1:2
Supply voltage	+3 V
Supply current	30 μA
Illumination mode	reflective
Character generator	external
Data interface	serial (C-bus)

DISPLAY MODE

Scale 1:1

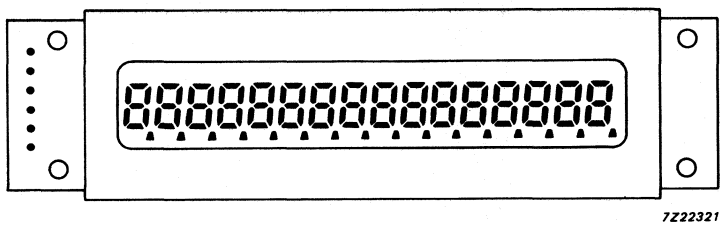


Fig.1 Universal display module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE
LTM233R-10	reflective

MECHANICAL DATA

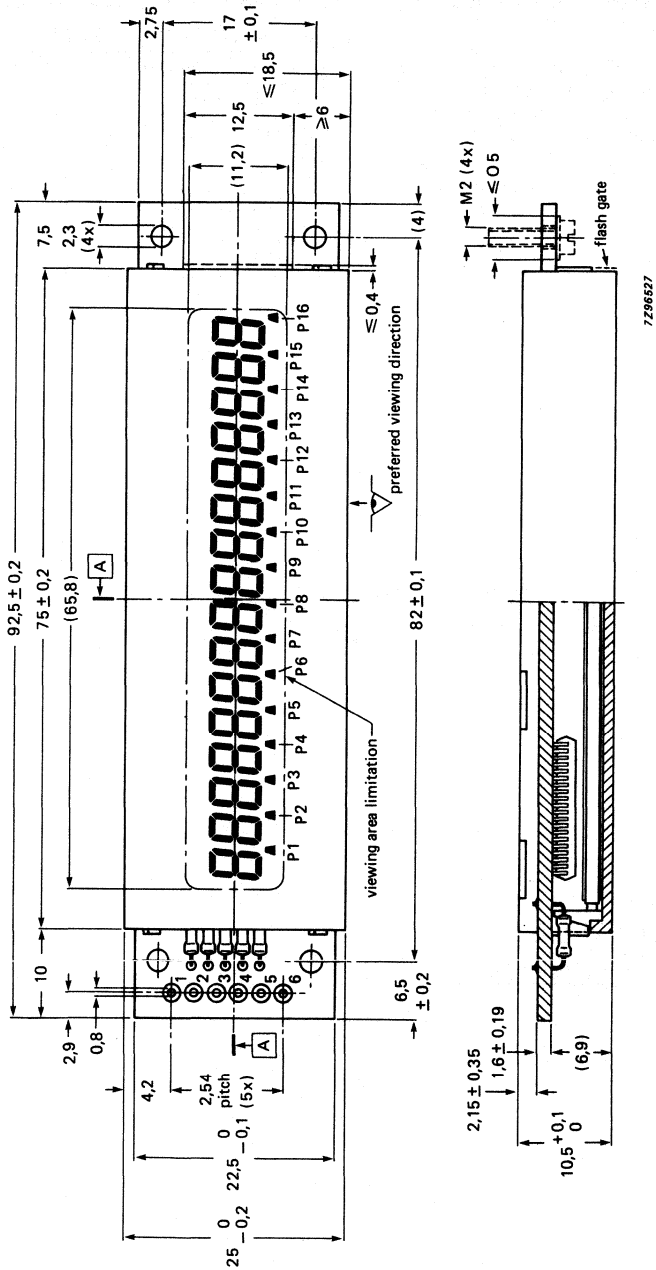


Fig. 2.

PIN DESCRIPTION

1	2	3	4	5	6
DLEN 1	DATA	DLEN 2	CLB	V_{DD}	GND

DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply voltage	V_{DD}	−0.3	–	8.0	V
HIGH level input voltage	V_{IH}	2.0	–	$V_{DD}+3$	V
LOW level input voltage	V_{IL}	−0.3	–	0.6	V

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
CLB pulse width HIGH	t_{WH}	3.0	–	–	μs
CLB pulse width LOW	t_{WL}	10.0	–	–	μs
Data set-up time DATA to CLB	t_{SUDA}	10.0	–	–	μs
Data hold time DATA to CLB	t_{HDDA}	10.0	–	–	μs
Enable set-up time DLEN to CLB	t_{SUEN}	3.0	–	–	μs
Disable set-up time CLB to DLEN	t_{SUDI}	10.0	–	–	μs
Set-up time load pulse DLEN to CLB	t_{SULD}	10.0	–	–	μs
Busy-time from load pulse to next start of transmission	t_{BUSY}	10.0	–	–	μs
Set-up time leading zero DATA to CLB	t_{SULZ}	10.0	–	–	μs

All times are measured with a voltage swing V_{IHmin} to V_{ILmin}.
Built in drivers: PCF2111 (x2)

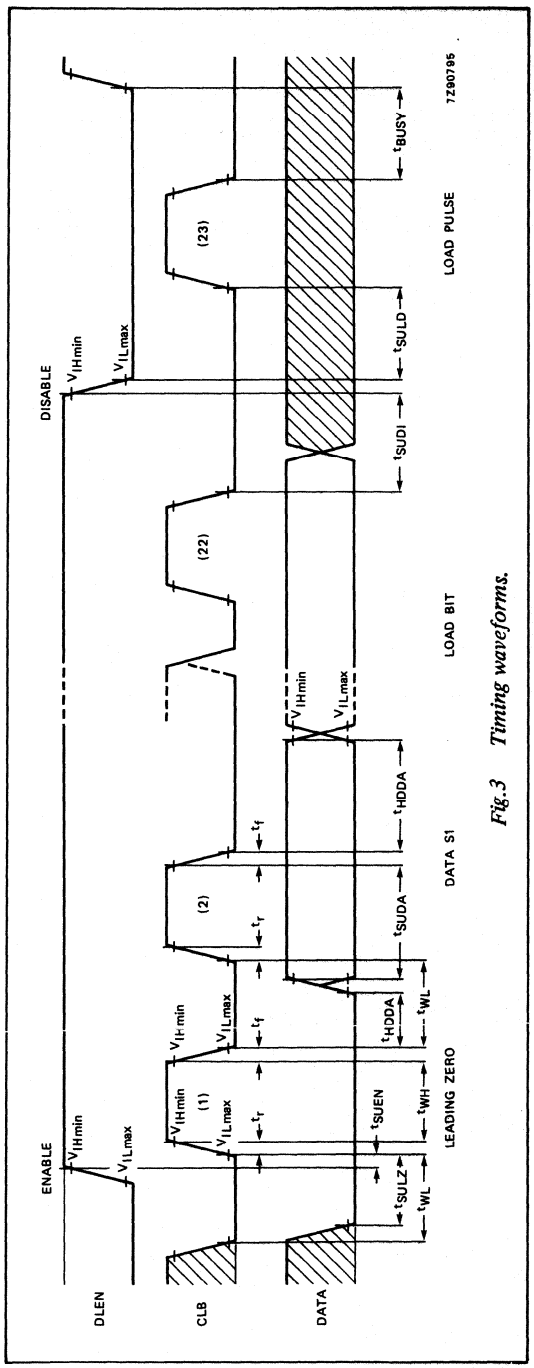


Fig.3 Timing waveforms.

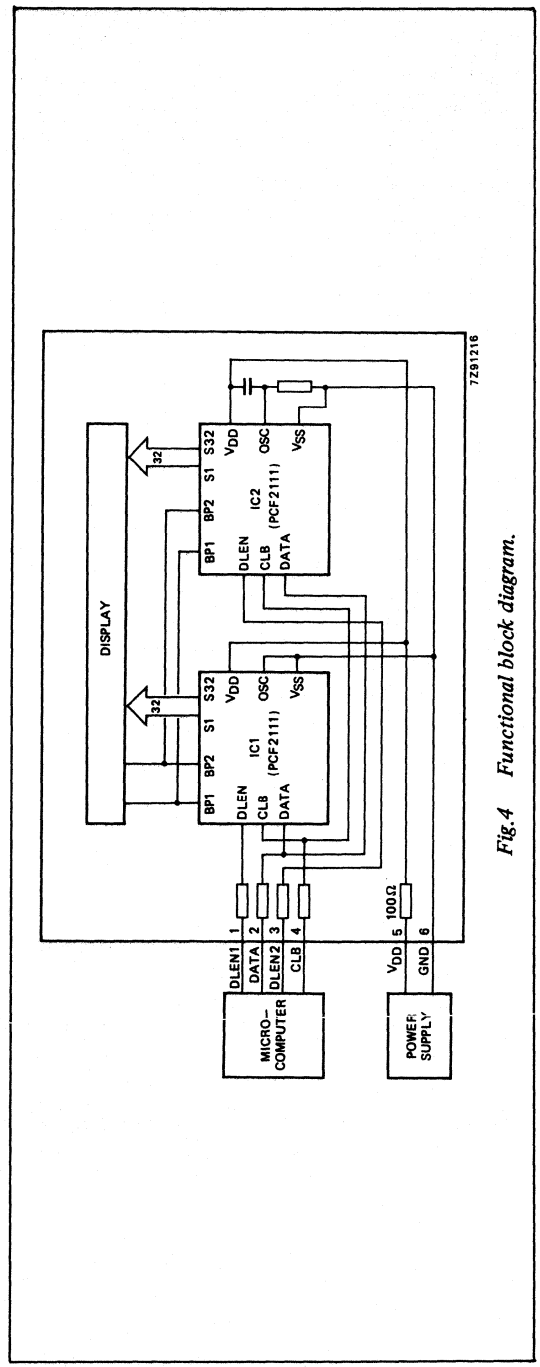


Fig.4 Functional block diagram.

Correspondence between IC-outputs and LCD-segments

Output	IC S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	BP 1	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d	f	e	p	d
Segment	BP 2	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c	a	g	b	c
	IC 1	1	1	1	1	2	2	2	2	3	3	3	3	4	4	4	4	5	5	5	5	6	6	6	6	7	7	7	7	8	8	8	8
Digit	IC 2	9	9	9	9	10	10	10	10	11	11	11	11	12	12	12	12	13	13	13	13	14	14	14	14	15	15	15	15	16	16	16	16

Liquid crystal display LTN111

MODULE DESCRIPTION

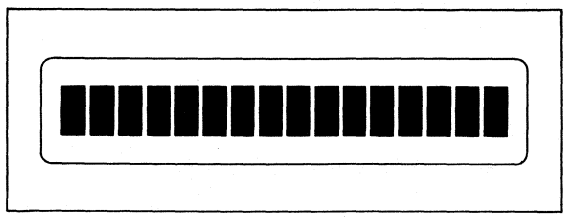
The LTN111R;F is a 5 X 7 dot, 16-character, 1-line dot matrix LCD module with LCD driver and controller LSI IC mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator with 160 characters and RAM display data with 8 characters. The module is capable of generating 160 fixed and 8 write by programme characters. The module operates from an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift.

QUICK REFERENCE DATA

Outline dimensions	80 X 36 X 12 mm
Viewing area	64.5 X 13.8 mm
Character format	5 X 7 dots and cursor
Character size	3.07 X 5.73 mm
Dot size (spacing 0.08 mm)	0.55 X 0.75 mm
Mass	≈ 25 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	7.5 mW
Illumination mode	reflective/transflective
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE

Scale 1:1



7Z22322

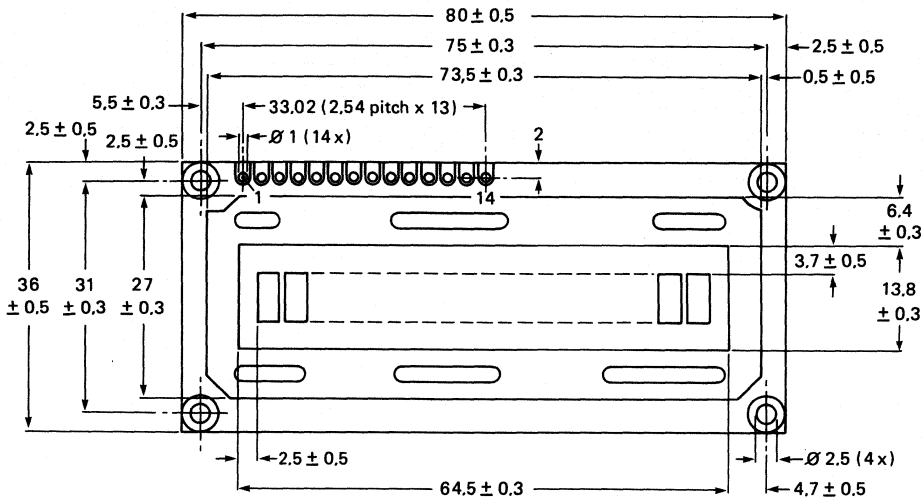
Fig.1 16-character, 1-line LCD module.

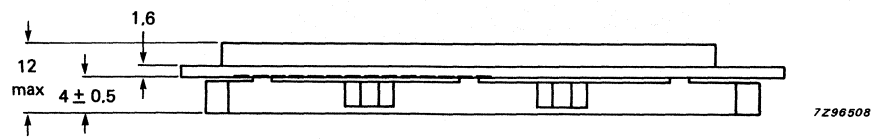
TYPE DEPENDENT DATA

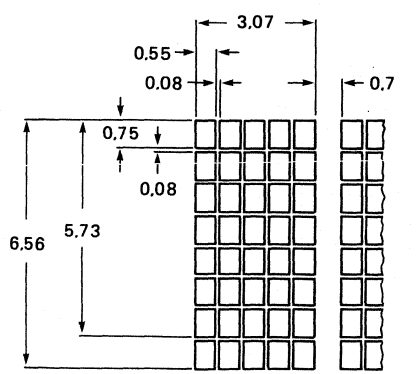
TYPE	ILLUMINATION MODE	TO BE USED WITH EL BACKLIGHT
LTN111R-10	reflective	–
LTN111F-10	transflective	LXL111-G

MECHANICAL DATA

Dimensions in mm







character pattern details 7Z96507

Fig.2 Module dimensions.

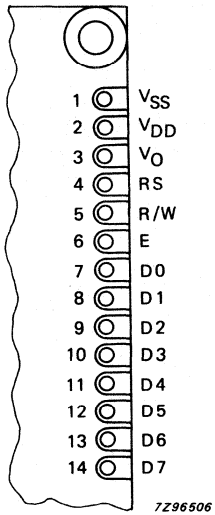


Fig.3 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as a busy flag output.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

Recommended connectors:
W-P5014, 5267-14A, FCN-724P014-AU/S, 65507-114.

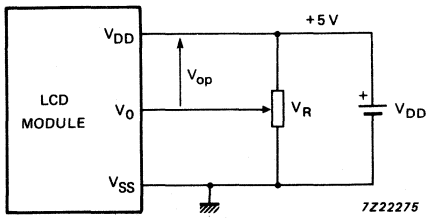


Fig. 4 Power supply.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	$V_{DD}-V_{SS}$	−0.3	–	7.0	V
LCD driver voltage ($V_{DD}-V_O$)	V_{OP}	0	–	13.5	V
Input voltage	V_I	−0.3	–	$V_{DD}+0.3$	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C ; all voltages refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}	4.75	5.0	5.25	V
contrast adjustment voltage	V_O	–	0.6	–	V
LOW level input voltage	V_{IL}	−0.03	–	0.6	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage $-I_{OH}$ = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	μA
Internal oscillating frequency	f_{osc}	–	250	–	kHz
Supply current (logic) see note	I_{DD}	–	1.5	2.0	mA
Power dissipation see note	P_d	–	7.5	10.0	mW

Note: V_{DD} = 5 V, V_O = 0 V.

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V ± 5% unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

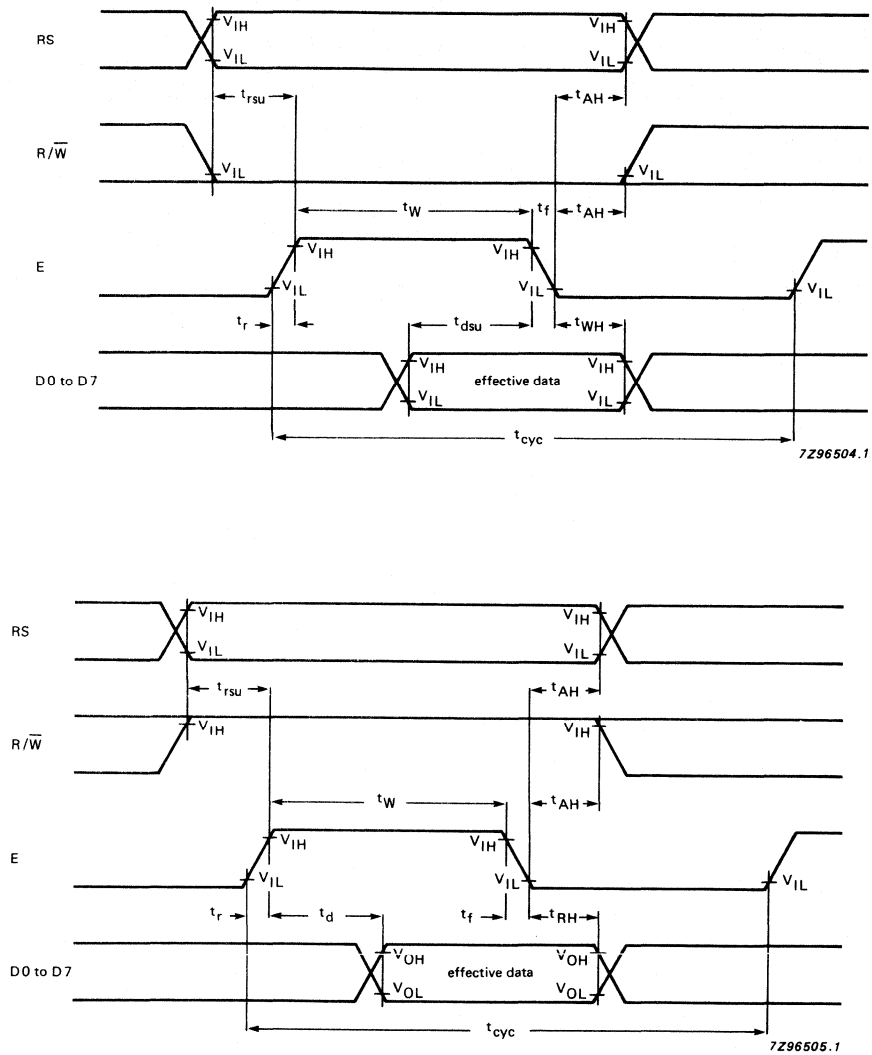


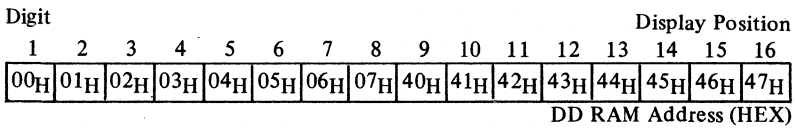
Fig.5 Timing waveforms.

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Where:

I/D	= 1:increment	I/D	= 0:decrement
S	= 1:display shift	S	= 0:display freeze
D	= 1:display on	D	= 0:display off
C	= 1:cursor on	C	= 0:cursor off
B	= 1:character at cursor position blinks	B	= 0:character at cursor position does not blink
S/C	= 1:display shift	S/C	= 0:cursor move
R/L	= 1:right shift	R/L	= 0:left shift
DL	= 1:8 bits	DL	= 0:4 bits
BF	= 1:during internal operation	BF	= 0:end of internal operation



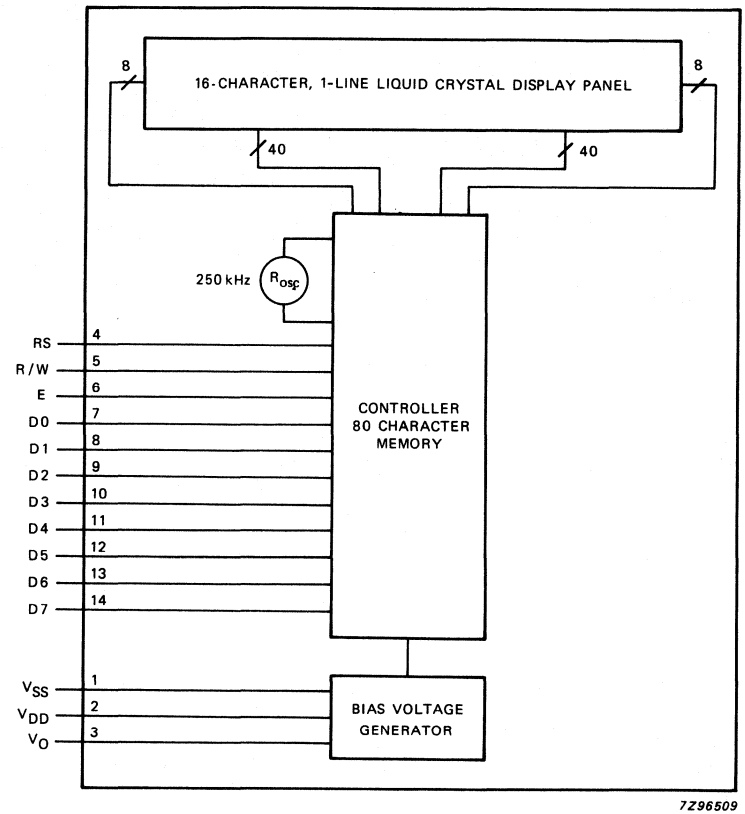
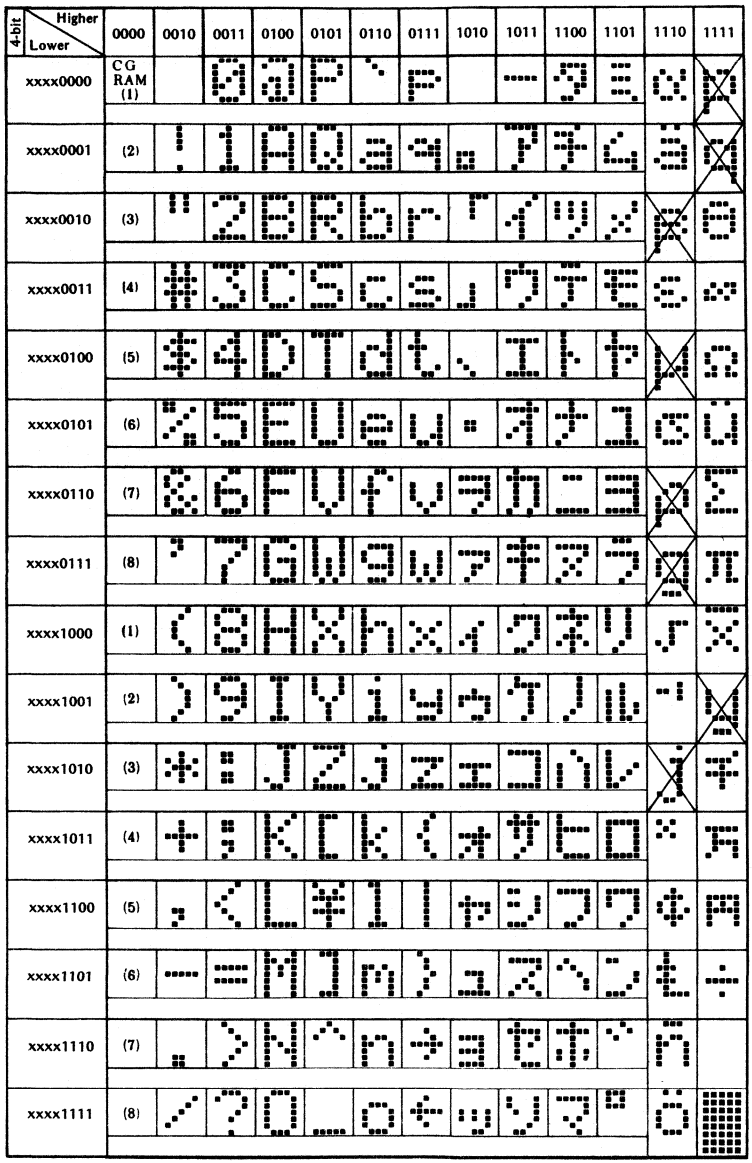


Fig. 6 Functional block diagram.

PHYSICAL ADDRESS

When the display address is not shifted it is as follows: the second lines 8 characters in logic correspond to the first line s 8 characters (right side) in display as the module is driven by a 1:16 multiplex rate.

INPUT CODE vs CHARACTER PATTERN



Note: CGRAM is a CHARACTER GENERATOR RAM having a storage function of character pattern which enable to change freely by users program.

Fig. 7 Display address.

Liquid crystal display LTN211

MODULE DESCRIPTION

The LTN211R; F is a 5 X 7 dot, 16-character, 2-line dot matrix LCD module with LCD driver and controller LSI ICs mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator and RAM display data. The module is capable of generating 168 alpha numeric and Japanese characters and has an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift. 160 of the characters are fixed and 8 are user programmable.

QUICK REFERENCE DATA

Outline dimensions	84 X 44 X 12 mm
Viewing area	61.0 X 15.8 mm
Character format	5 X 7 dots and cursor
Character size	2.96 X 4.86 mm
Dot size (spacing 0.04 mm)	0.56 X 0.66 mm
Mass	≈ 28 g
Drive method	MUX 1:16
Supply voltage	+5 V
Power consumption	7.5 mW
Illumination mode	reflective/transflective
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE

Scale 1:1

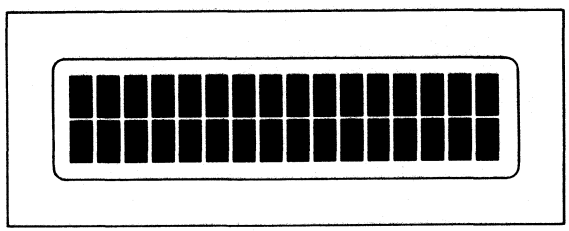


Fig.1 16-character, 2-line LCD module.

TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	TO BE USED WITH EL BACKLIGHT
LTN211R-10	reflective	–
LTN211F-10	transflective	LXL211-G

MECHANICAL DATA

Dimensions in mm

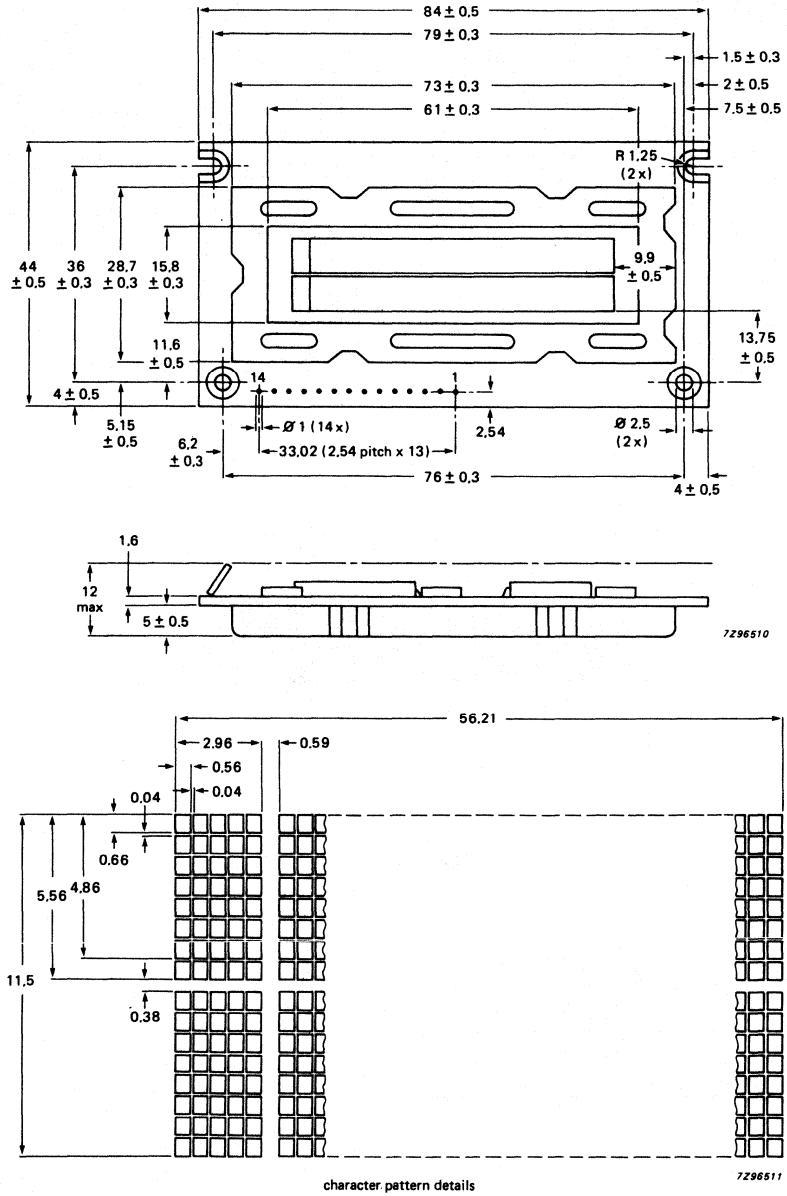


Fig.2 Module dimensions.

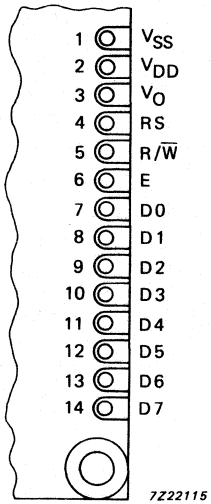


Fig.3 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O between 0 and 5 V.
2. D7 doubles as a busy flag output.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, pins D0 to D3 are not used.

Recommended connectors:
W-P5014, 5267-14A, FCN-724P014-AU/S, 65507-114.

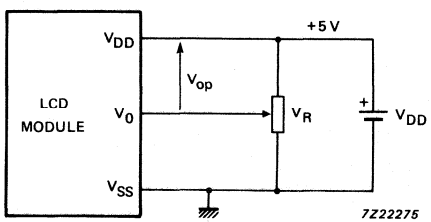


Fig. 4 Power supply.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{DD}	−0.3	–	7.0	V
LCD driver voltage ($V_{DD}-V_O$)	V_{OP}	0	–	13.5	V
Input voltage	V_I	−0.3	–	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all values refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	–	0.6	–	V
LOW level input voltage	V_{IL}	−0.03	–	0.6	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage $-I_{OH}$ = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	μA
Internal oscillating frequency	f_{osc}	–	250	–	kHz
Supply current (logic) see note	I_{DD}	–	1.6	2.2	mA
Power dissipation see note	P_d	–	8.0	11.0	mW

Note: V_{DD} = 5 V, V_O = 0 V.

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C, V_{DD} = 5 V ± 5% unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

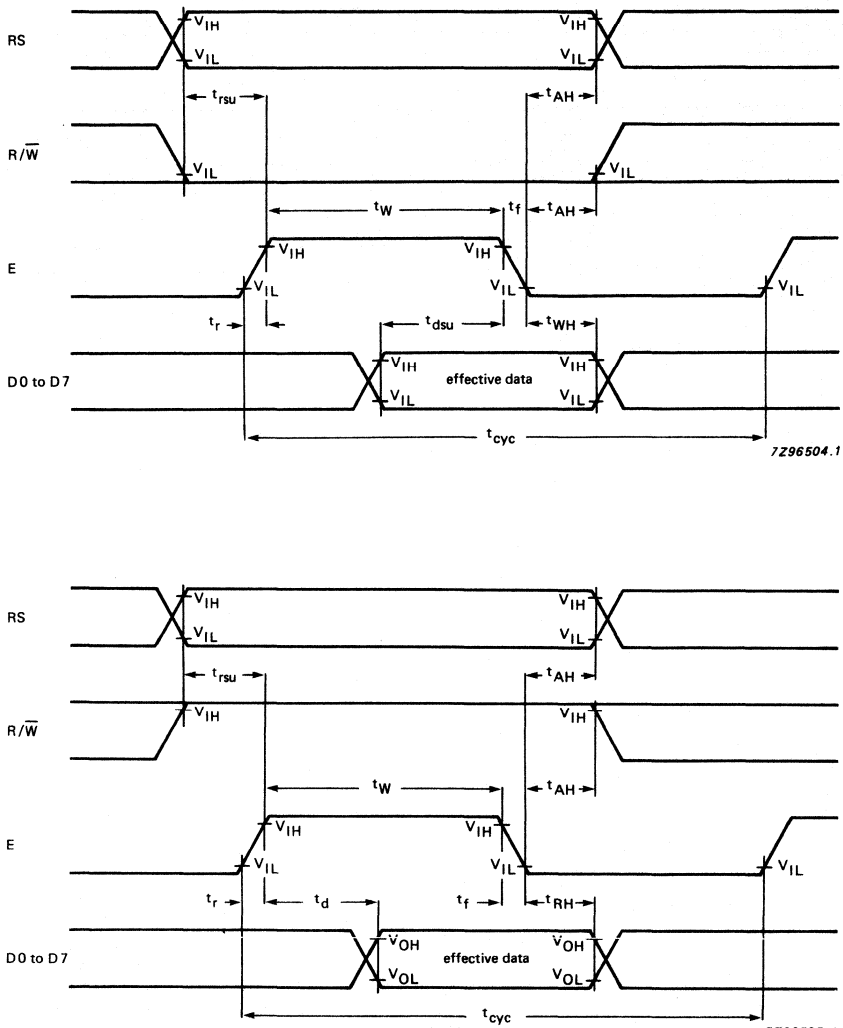


Fig.5 Timing waveforms.

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Where:

I/D = 1:increment	I/D = 0:decrement
S = 1:display shift	S = 0:display freeze
D = 1:display on	D = 0:display off
C = 1:cursor on	C = 0:cursor off
B = 1:character at cursor position blinks	B = 0:character at cursor position does not blink
S/C = 1:display shift	S/C = 0:cursor move
R/L = 1:right shift	R/L = 0:left shift
DL = 1:8 bits	DL = 0:4 bits
BF = 1:during internal operation	BF = 0:end of internal operation

Display Position

Digit	1	2	3	4	5	6	7	8	9		16
Line 1	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	.....	$0F_H$
Line 2	40_H	41_H	42_H	43_H	44_H	45_H	46_H	47_H	48_H	.....	$4F_H$

DD RAM Address (HEX)

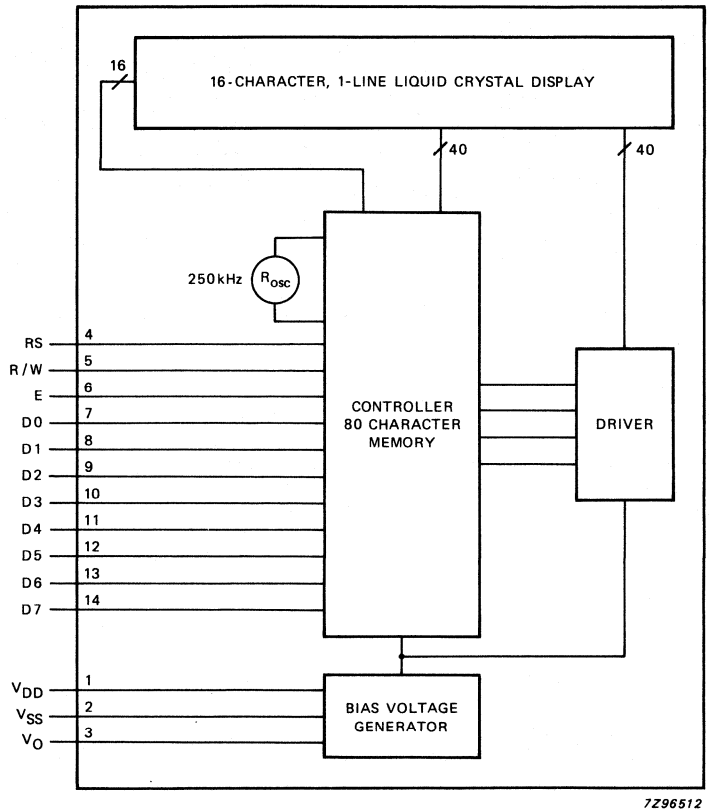
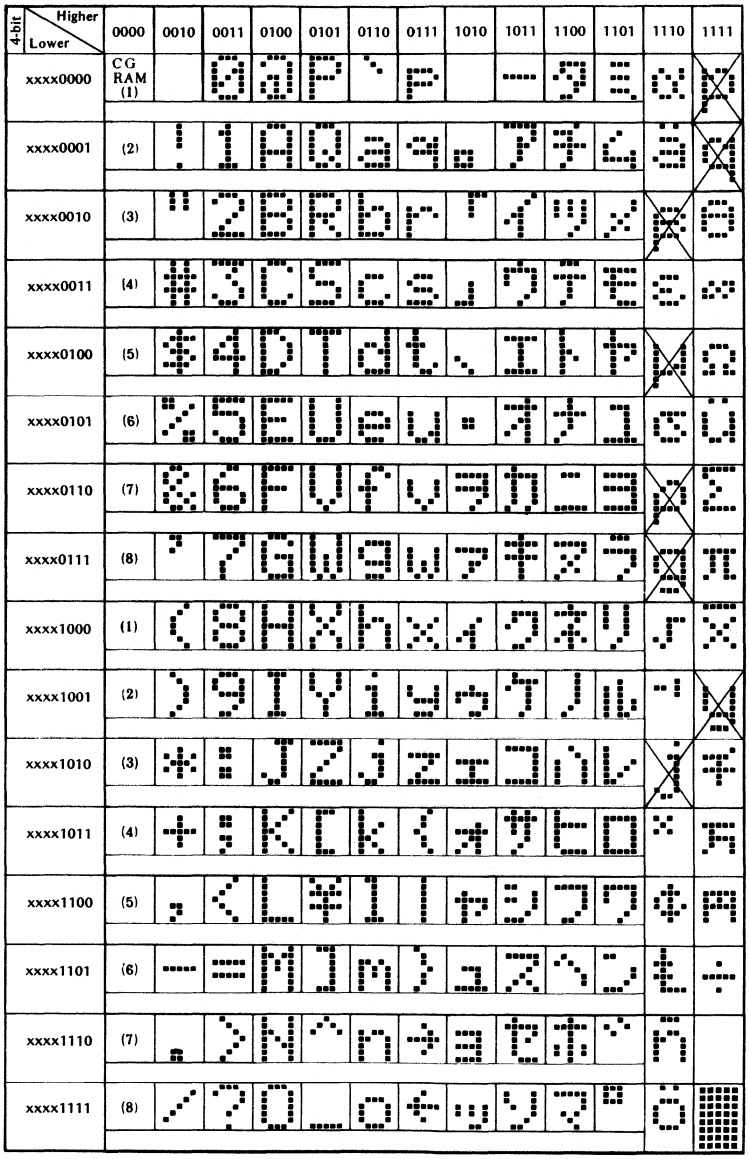


Fig. 6 Functional block diagram.

INPUT CODE vs CHARACTER PATTERN



Note: CGRAM is a CHARACTER GENERATOR RAM having a storage function of character pattern which enable to change freely by users program.

Fig. 7 Display address.

Liquid crystal display LTN241

MODULE DESCRIPTION

The LTN241R-10 is a 5 X 7 dot, 40-character, 2-line dot matrix LCD module with LCD driver and controller LSI ICs mounted on a single printed circuit board. The LSI controller incorporates a ROM-based character generator and RAM display data. The module is capable of generating 168 alpha numeric and Japanese characters and has an extensive instruction set: display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift and display shift. 160 of the characters are fixed and 8 are user programmable.

QUICK REFERENCE DATA

Outline dimensions	182 X 33.5 X 11 mm
Viewing area	154.4 X 15.8 mm
Character format	5 X 7 dots and cursor
Character size	3.2 X 4.85 mm
Dot size (spacing 0.05 mm)	0.6 X 0.65 mm
Mass	≈ 65 g
Drive method	MUX 1:16
Supply voltage	+5 V; −5 V
Power consumption	11 mW
Illumination mode	reflective
Character generator	built in
Data interface	parallel 4 or 8 bits

DISPLAY MODE

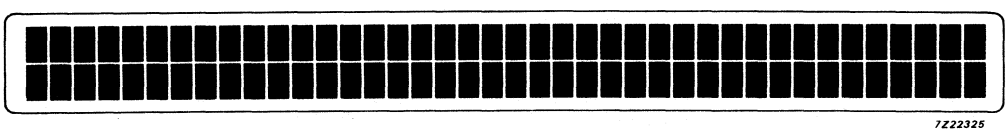


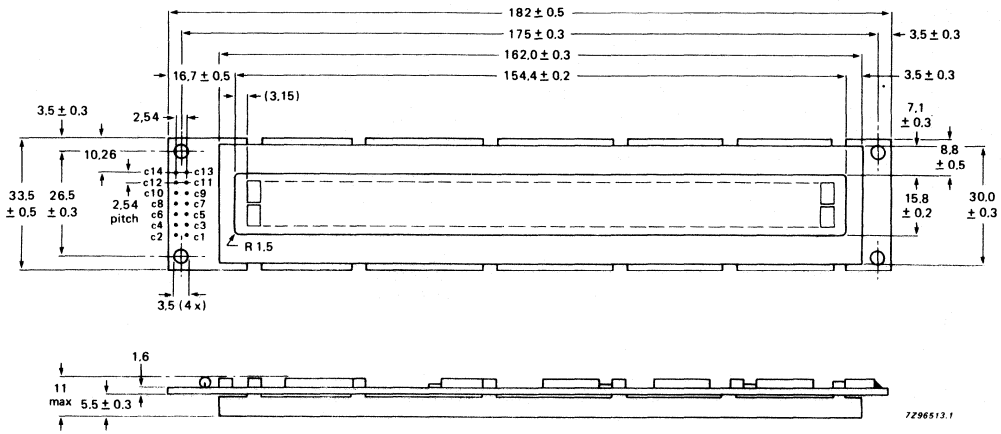
Fig.1 40-character, 2-line LCD module.

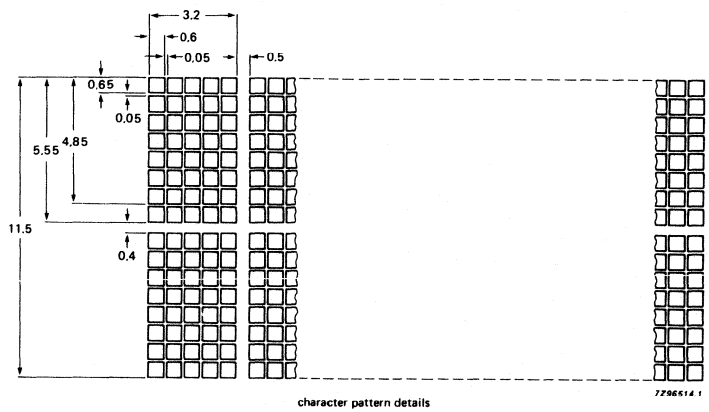
TYPE DEPENDENT DATA

TYPE	ILLUMINATION MODE	TO BE USED WITH EL BACKLIGHT
LTN241R-10	reflective	–

MECHANICAL DATA

Dimensions in mm





character pattern details

Fig. 2 Module dimensions.

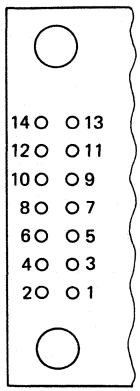


Fig.3 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{SS}	ground
2	V_{DD}	power supply (logic)
3	V_O	contrast adjustment voltage
4	RS	register select
5	R/W	read/write
6	E	enable
7	D0	I/O data LSB
8	D1	I/O data 2nd bit
9	D2	I/O data 3rd bit
10	D3	I/O data 4th bit
11	D4	I/O data 5th bit
12	D5	I/O data 6th bit
13	D6	I/O data 7th bit
14	D7	I/O data MSB

Notes to pin description

1. Contrast is adjusted by varying the voltage V_O
2. D7 doubles as a busy flag output.
3. When the module is interfaced with a microprocessor with 4-bit parallel outputs, Pins D0 to D3 are not used.

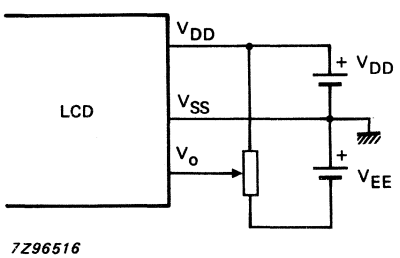


Fig. 4 Power supply.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage V_{SS} = 0 V	V_{DD}	−0.3	–	7.0	V
LCD driver voltage	$V_{DD}-V_O$	0	–	13.5	V
Input voltage V_{SS} = 0 V	V_I	−0.3	–	V_{DD}+0.3	V
Storage temperature	T_{stg}	−25	–	+70	°C
Operating ambient temperature	T_{amb}	0	–	+50	°C

OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V_{DD} = 5 V; all voltage values refer to V_{SS}; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (logic)	V_{DD}	4.75	5.0	5.25	V
Contrast adjustment voltage	V_O	–	− 0.5	–	V
LOW level input voltage	V_{IL}	−0.03	–	0	V
HIGH level input voltage	V_{IH}	2.2	–	V_{DD}	V
LOW level output voltage I_{OL} = 1.2 mA	V_{OL}	–	–	0.4	V
HIGH level output voltage $-I_{OH}$ = 0.205 mA	V_{OH}	2.4	–	–	V
Input leakage current	I_I	–	–	1.0	μA
Internal oscillating frequency	f_{osc}	–	160	–	kHz
Supply current (logic) see note	I_{DD}	–	2.2	3.2	mA
Power dissipation see note	P_d	–	11.0	16.0	mW

Note: V_{DD} = 5 V; V_O = 0 V.

TIMING CHARACTERISTICS

T_{amb} = 0 to 50 °C. V_{DD} = 5 V ± 5% unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	t_{cyc}	1000	–	–	ns
Enable pulse width	t_W	450	–	–	ns
Rise time	t_r	–	–	25	ns
Fall time	t_f	–	–	25	ns
Register select set-up time	t_{rsu}	140	–	–	ns
Read and write set-up time	t_{su}	140	–	–	ns
Data set-up time	t_{dsu}	195	–	–	ns
Data delay time	t_d	–	–	320	ns
Address hold time	t_{AH}	10	–	–	ns
Data hold time write	t_{WH}	10	–	–	ns
Data hold time read	t_{RH}	20	–	–	ns

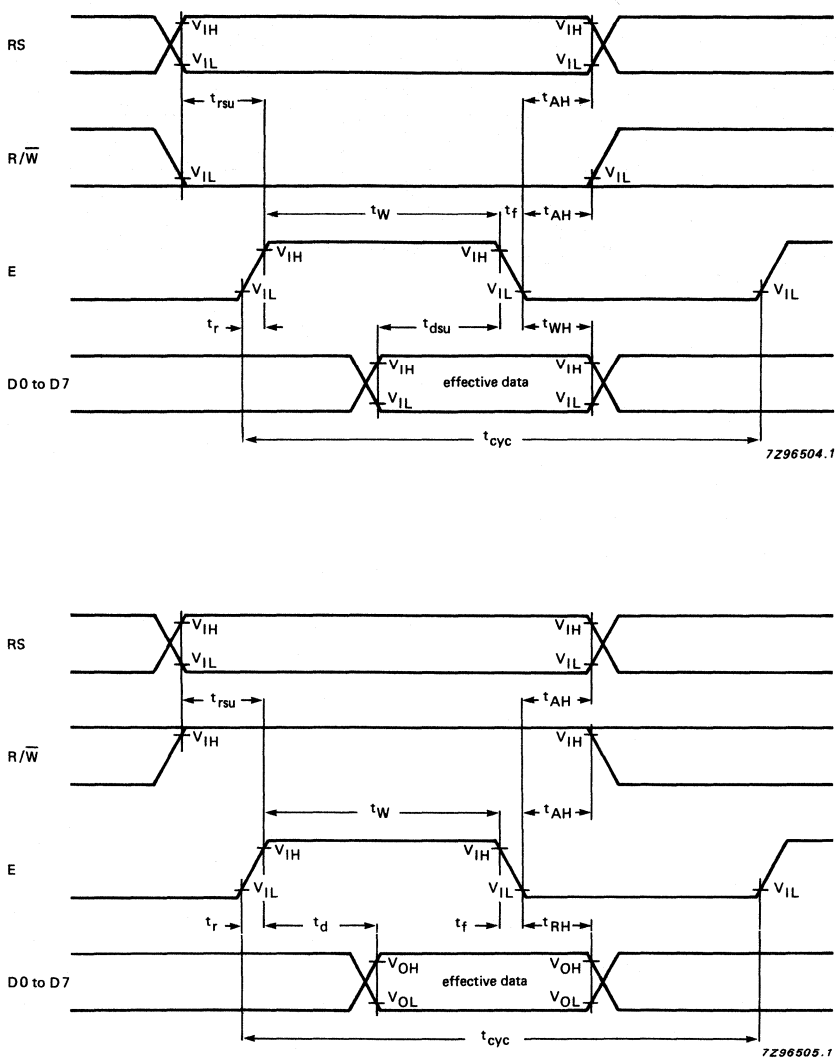


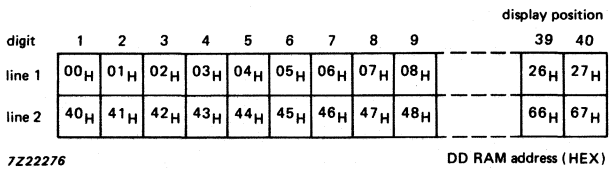
Fig.5 Timing waveforms.

Table 1 Instruction set

INSTRUCTION \ ADDRESSES	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Display clear	0	0	0	0	0	0	0	0	0	1
Cursor home	0	0	0	0	0	0	0	0	1	*
Entry mode set	0	0	0	0	0	0	0	1	I/D	S
Display on/off control	0	0	0	0	0	0	1	D	C	B
Cursor display shift	0	0	0	0	0	1	S/C	R/L	*	*
Function set	0	0	0	0	1	DL	1	0	*	*
CG RAM address set	0	0	0	1	A_{CG}					
DD RAM address set	0	0	1	A_{DD}						
Busy flag/address read	0	1	BF	AC						
CG RAM/DD RAM data write	1	0	write data							
CG RAM/DD RAM data read	1	1	read data							

Where:

I/D	= 1:increment	I/D	= 0:decrement
S	= 1:display shift	S	= 0:display freeze
D	= 1:display on	D	= 0:display off
C	= 1:cursor on	C	= 0:cursor off
B	= 1:character at cursor position blinks	B	= 0:character at cursor position does not blink
S/C	= 1:display shift	S/C	= 0:cursor move
R/L	= 1:right shift	R/L	= 0:left shift
DL	= 1:8 bits	DL	= 0:4 bits
BF	= 1:during internal operation	BF	= 0:end of internal operation



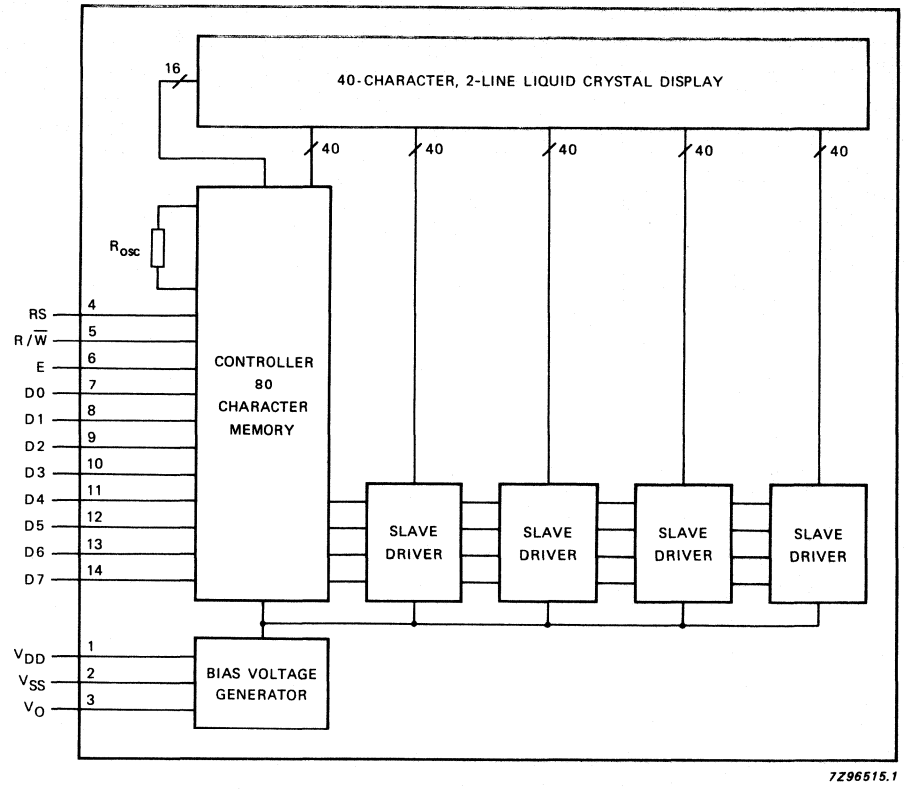
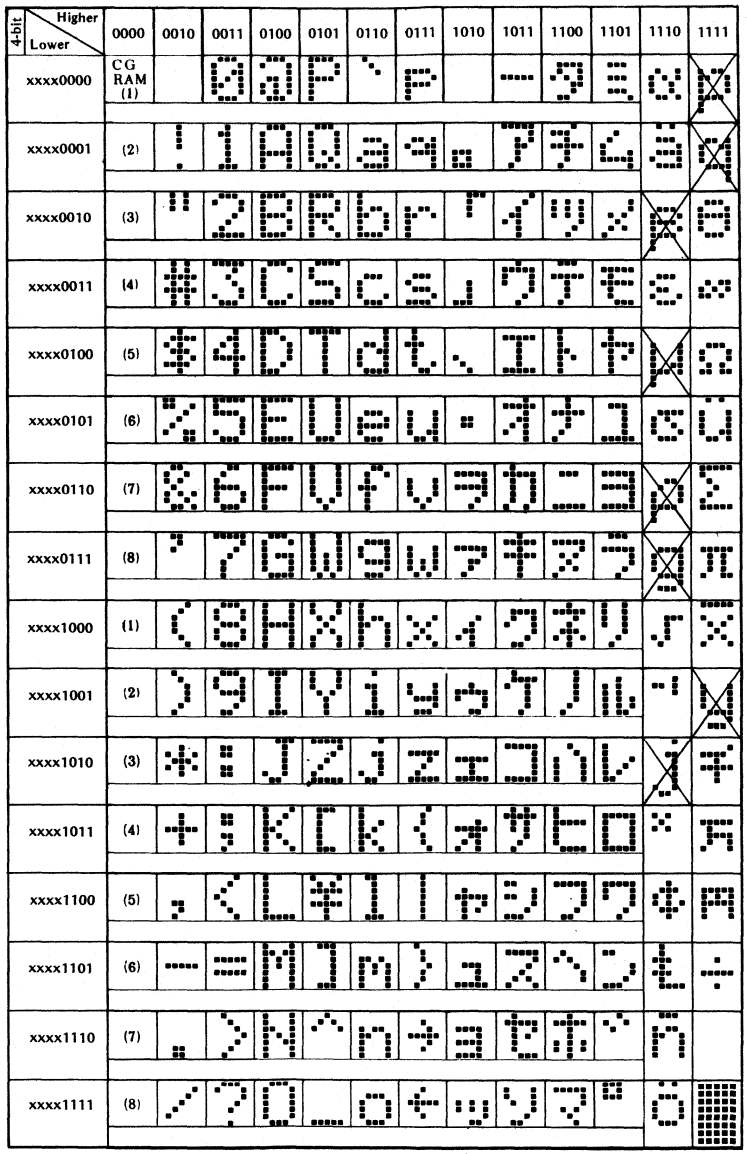


Fig. 6 Functional block diagram.

INPUT CODES vs CHARACTER PATTERN



Note: CGRAM is a CHARACTER GENERATOR RAM having a storage function of character pattern which enable to change freely by users program.

Fig. 7 Display address.

Driver ICs for LCD

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT-117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT-129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).
PCF2112T:

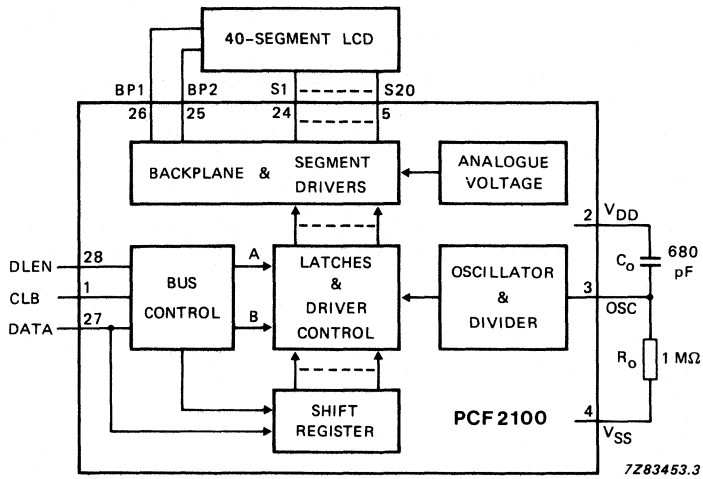


Fig. 1 Block diagram; PCF2100

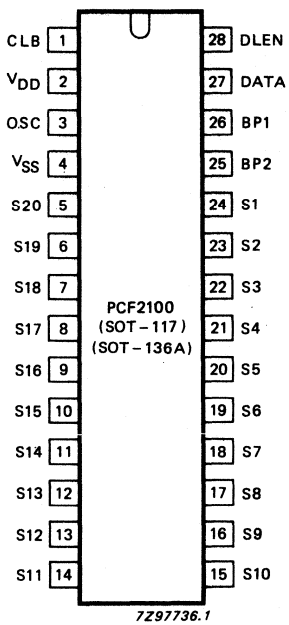


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
27	DATA	data line (CBUS)
28	DLEN	data line enable (CBUS)

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

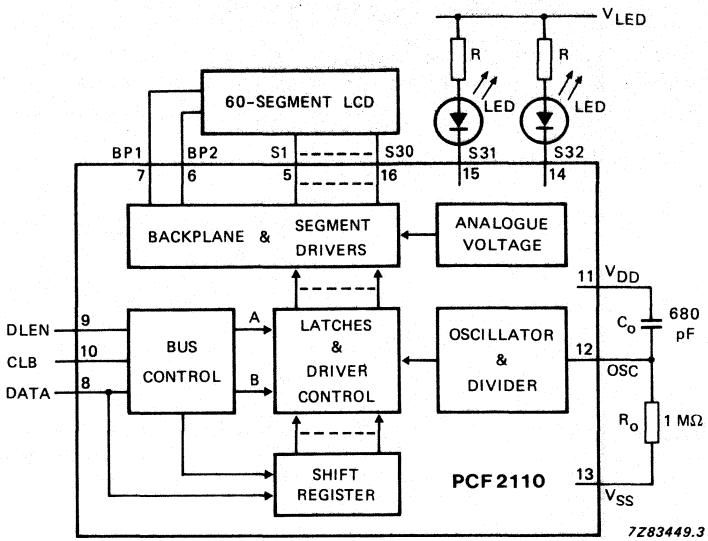


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

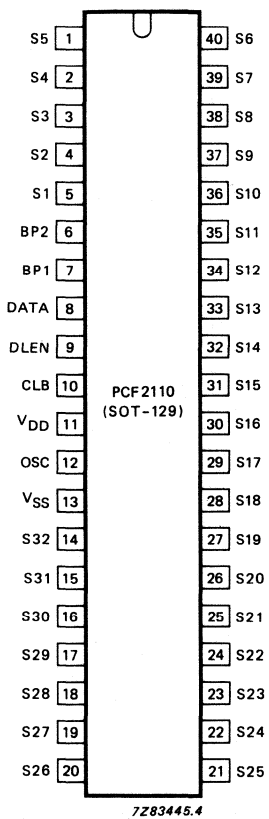


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

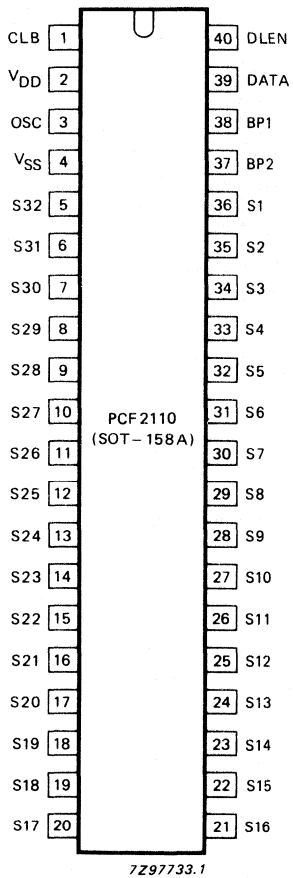


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

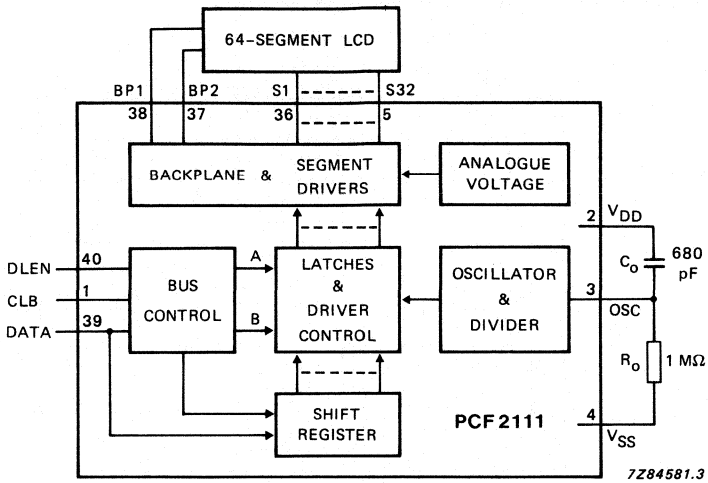


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

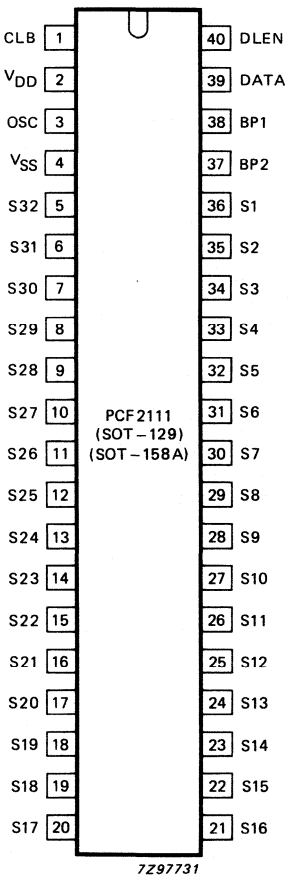


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line } CBUS
40	DLEN	data line enable } CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

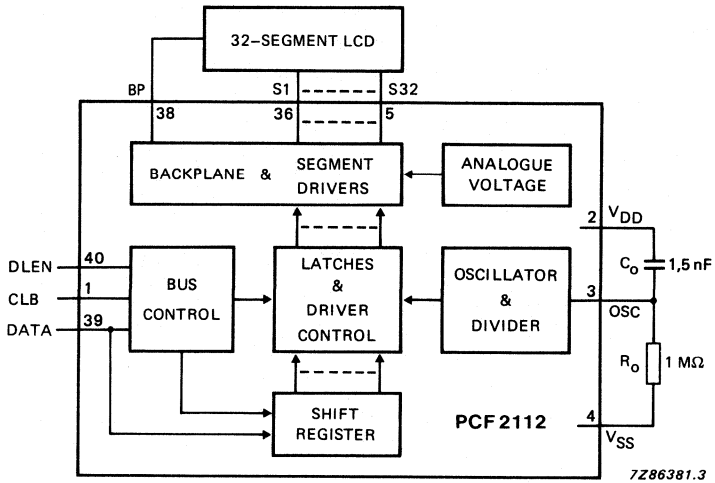


Fig. 8 Block diagram; PCF2112

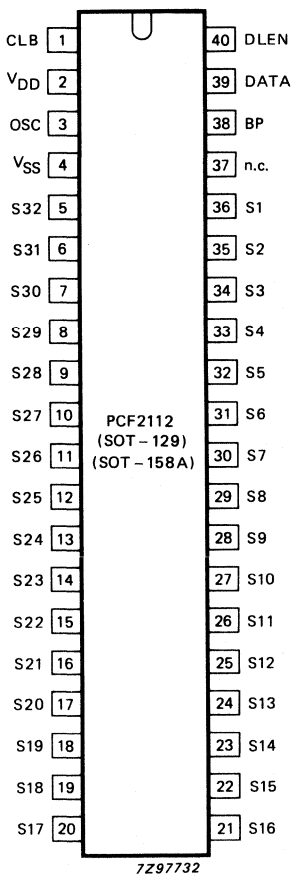


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

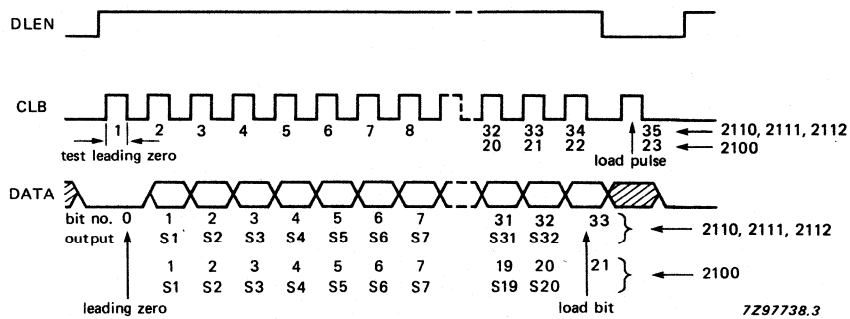


Fig. 10 CBUS data format.

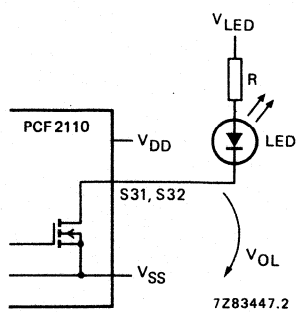


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

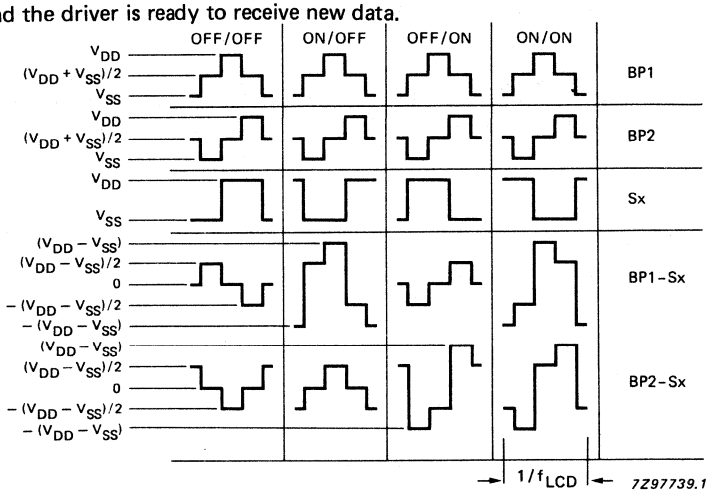


Fig. 12 Timing diagram (except PCF2112).

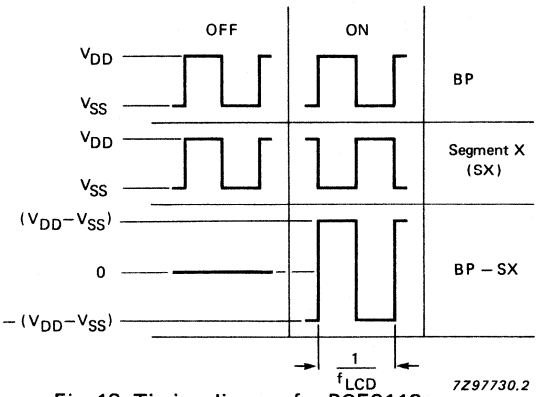


Fig. 13 Timing diagram for PCF2112.

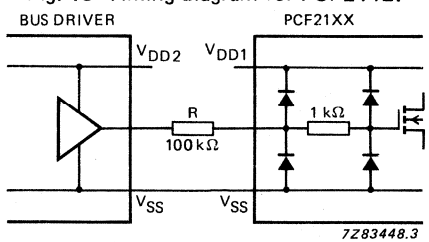
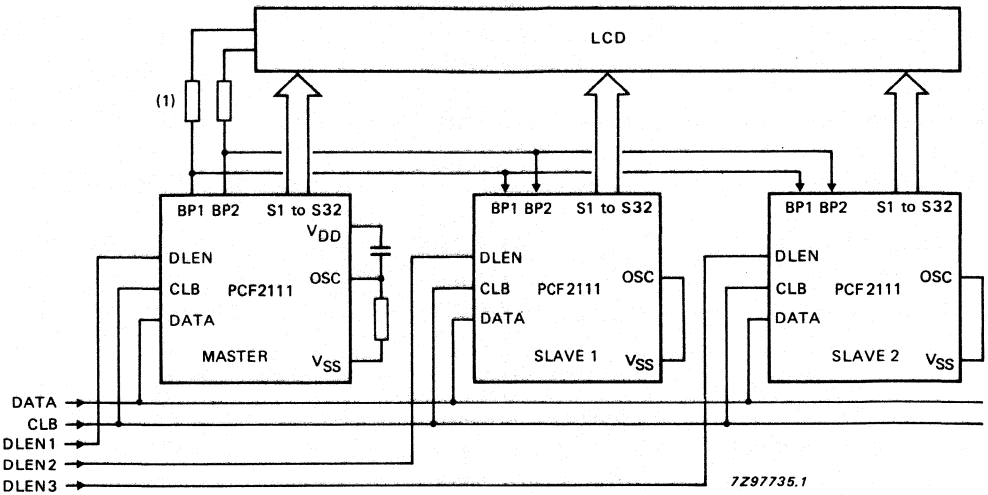


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu$A.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

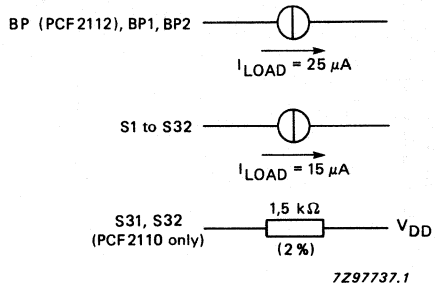


Fig. 16 Test loads.

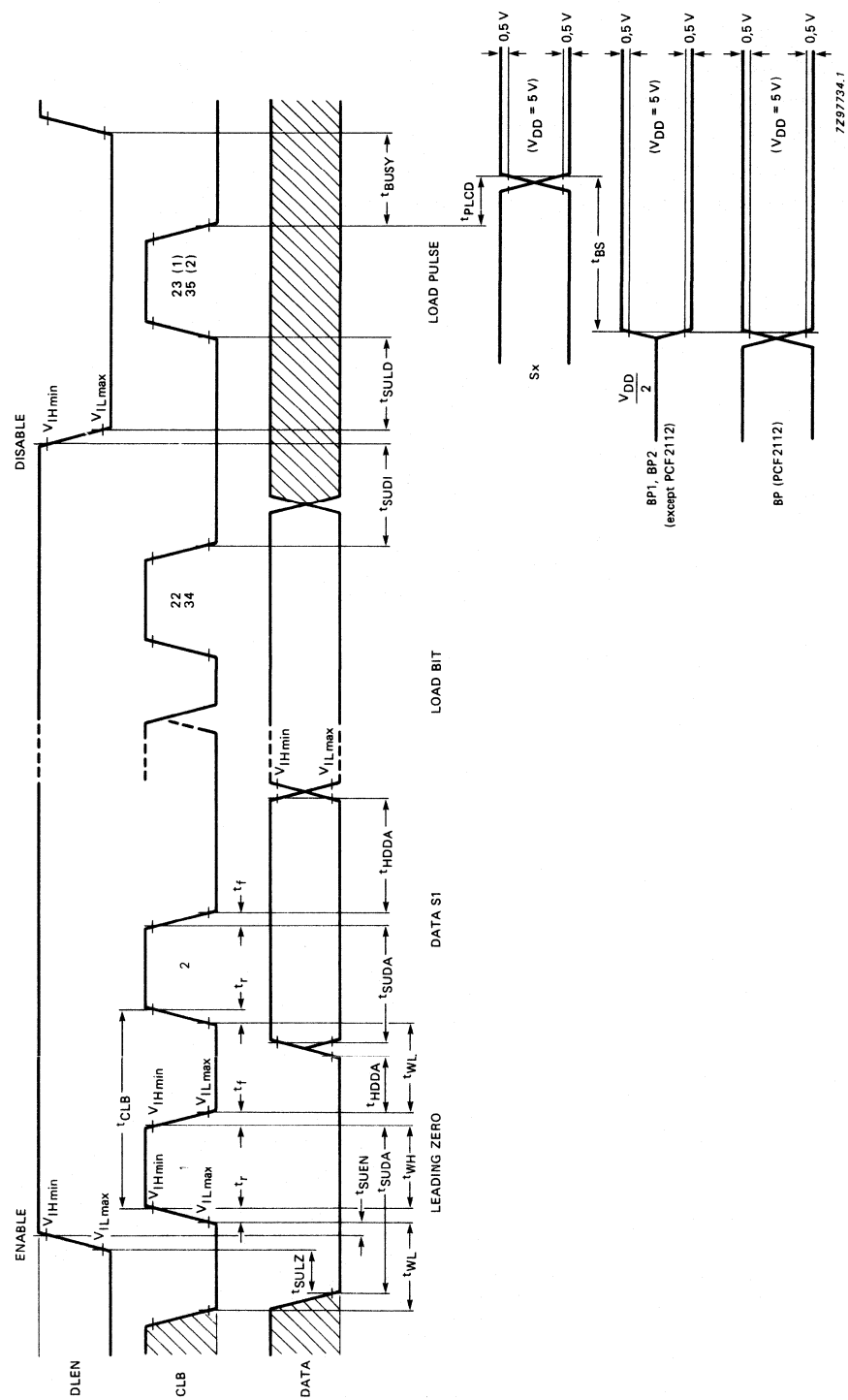


Fig. 17 CBUS timing.

(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

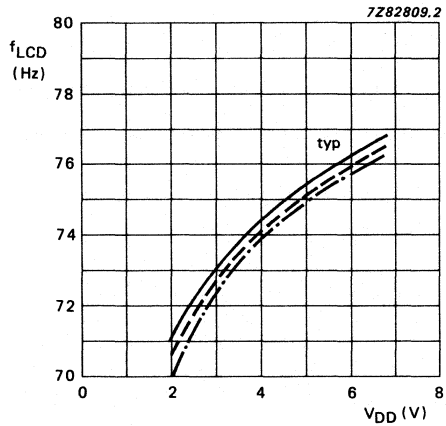


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

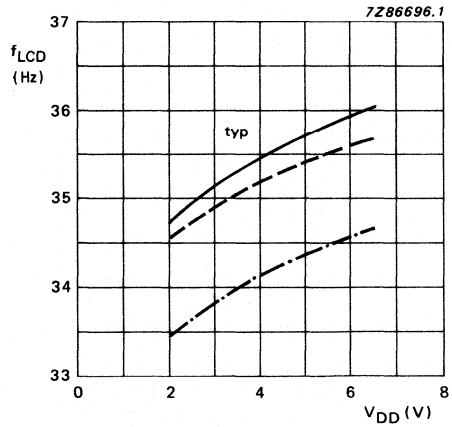


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

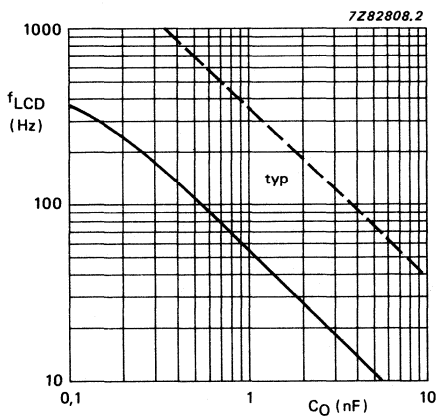


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

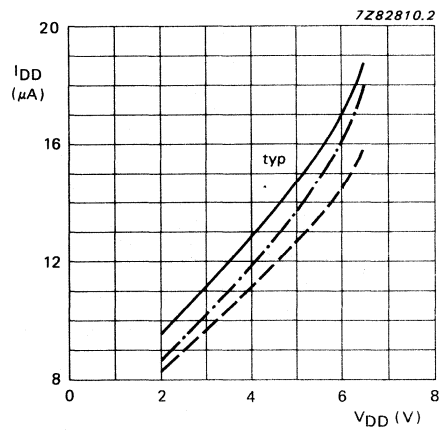


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

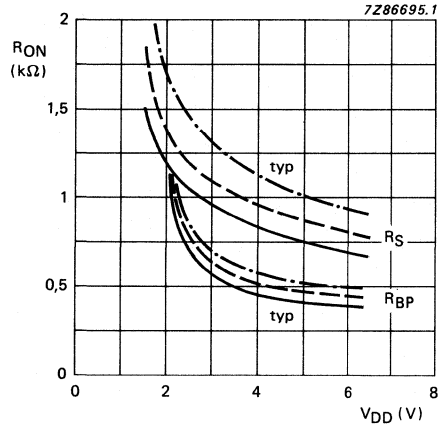


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

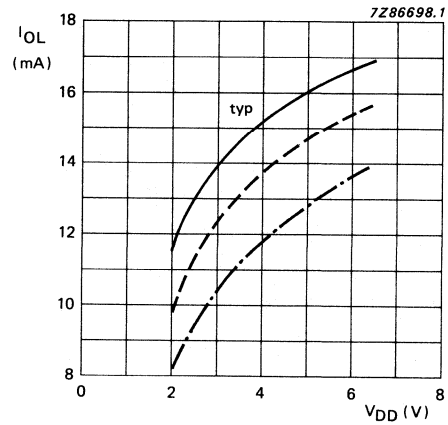


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT-129).
PCF8566T: 40-lead mini-pack (VSO-40; SOT-158A).

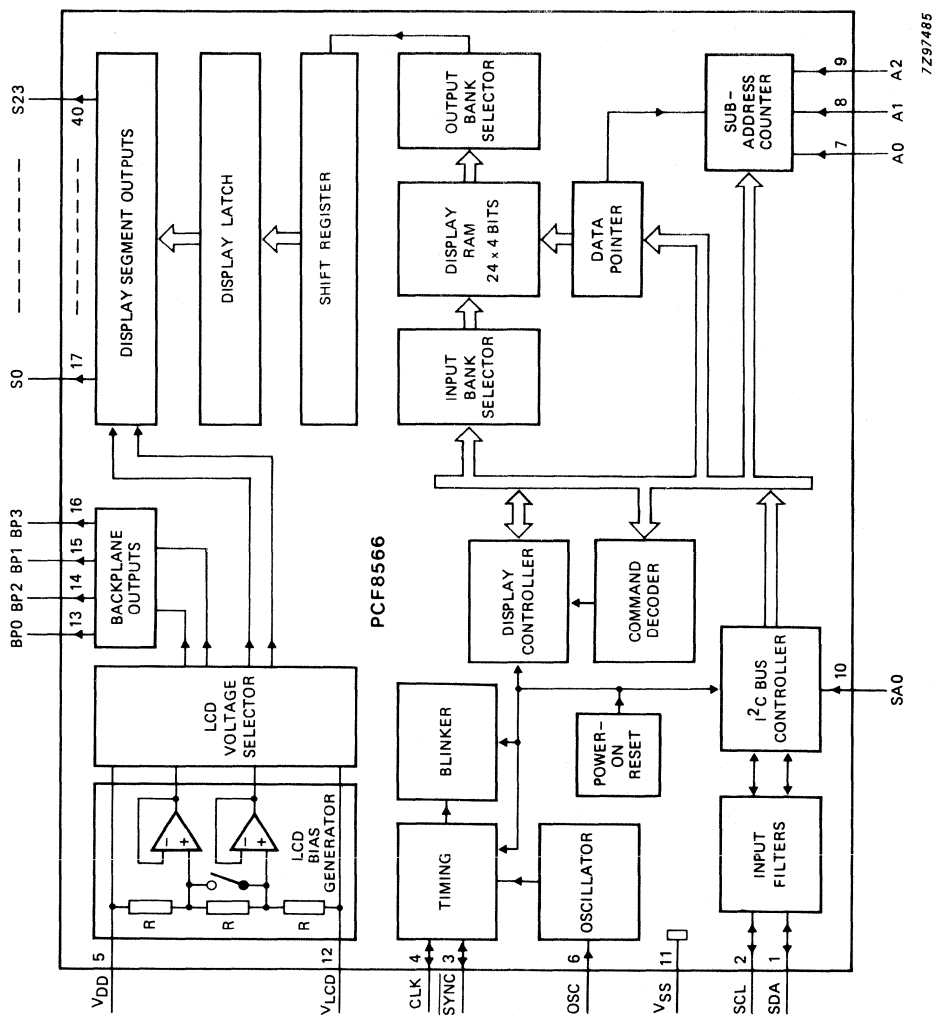


Fig. 1 Block diagram.

DEVELOPMENT DATA

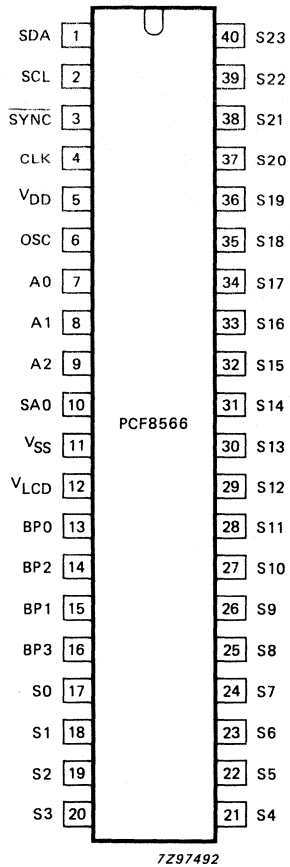


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17	S0	LCD segment outputs
to	to	
40	S23	

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

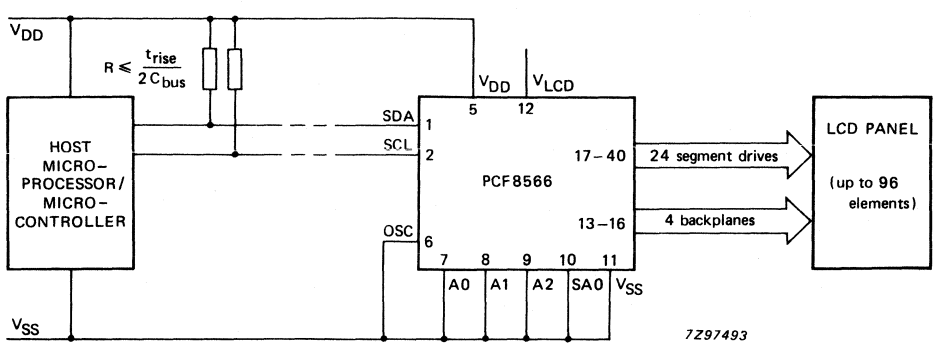


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

DEVELOPMENT DATA

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

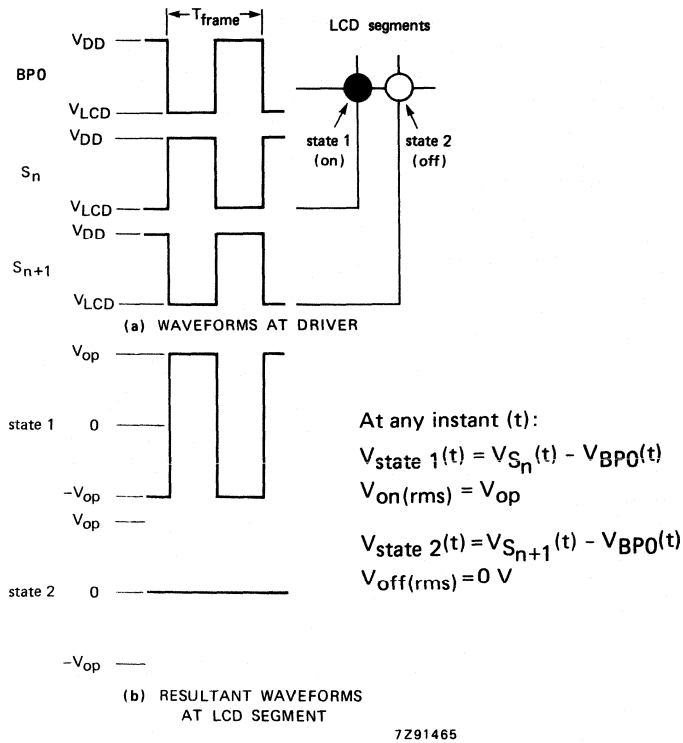


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

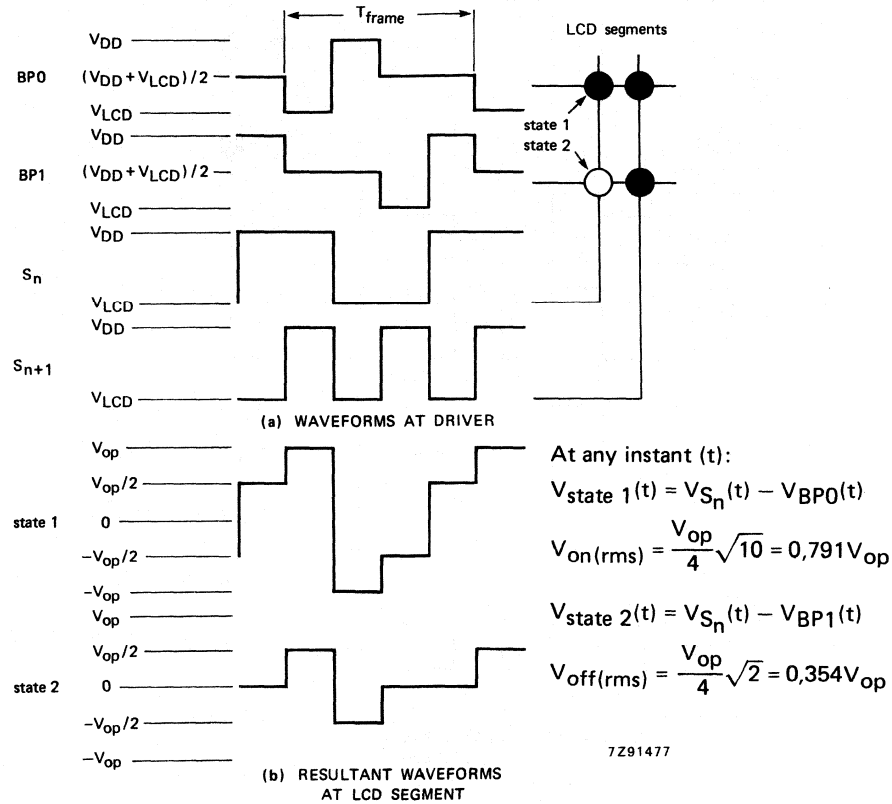


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

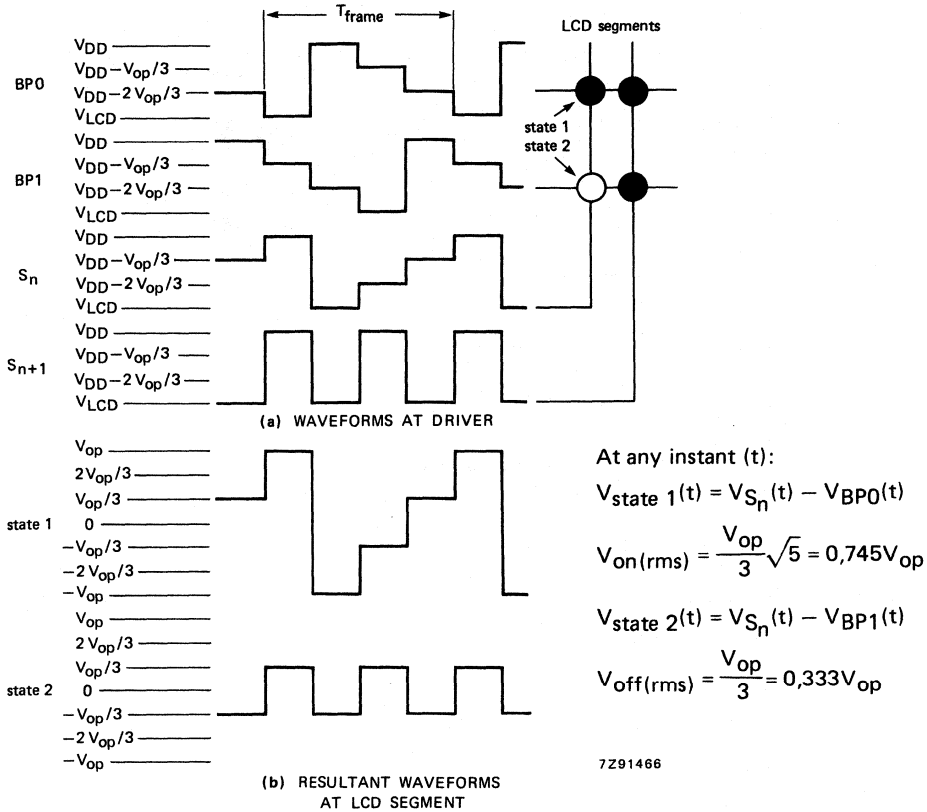


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

DEVELOPMENT DATA

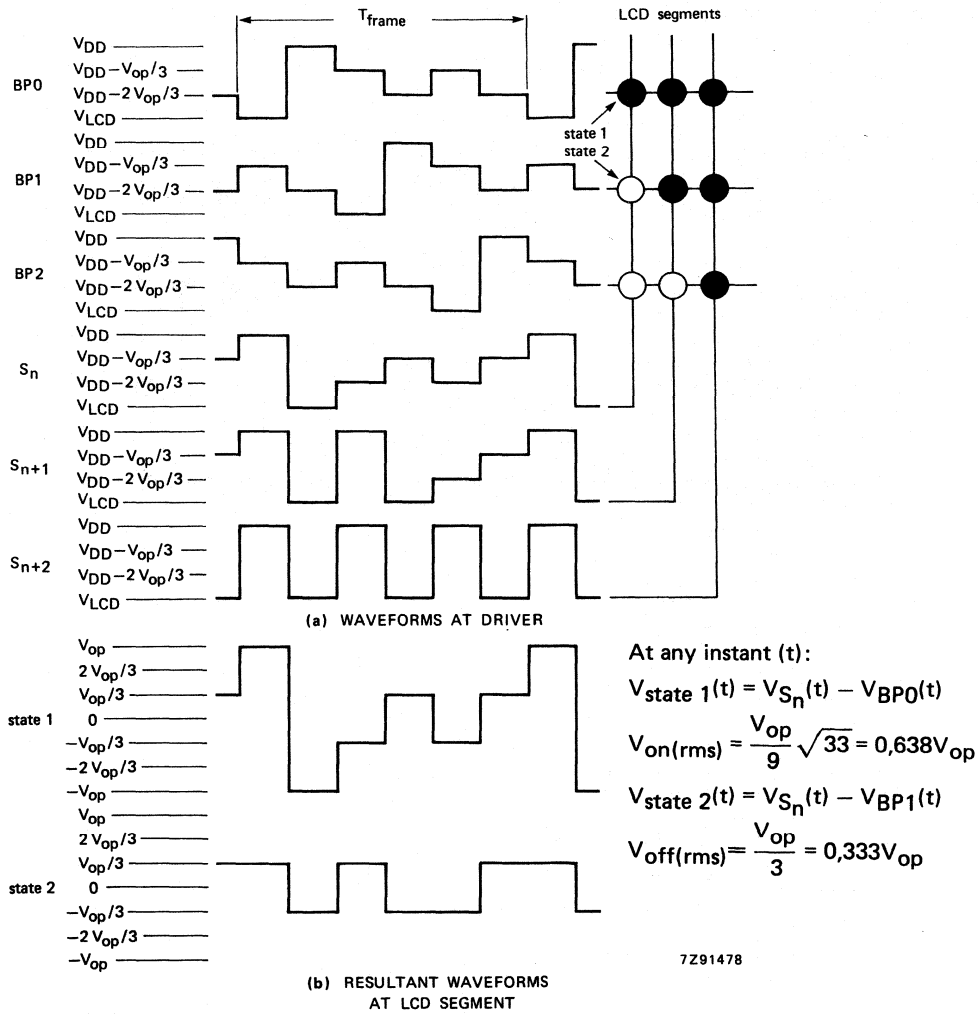


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

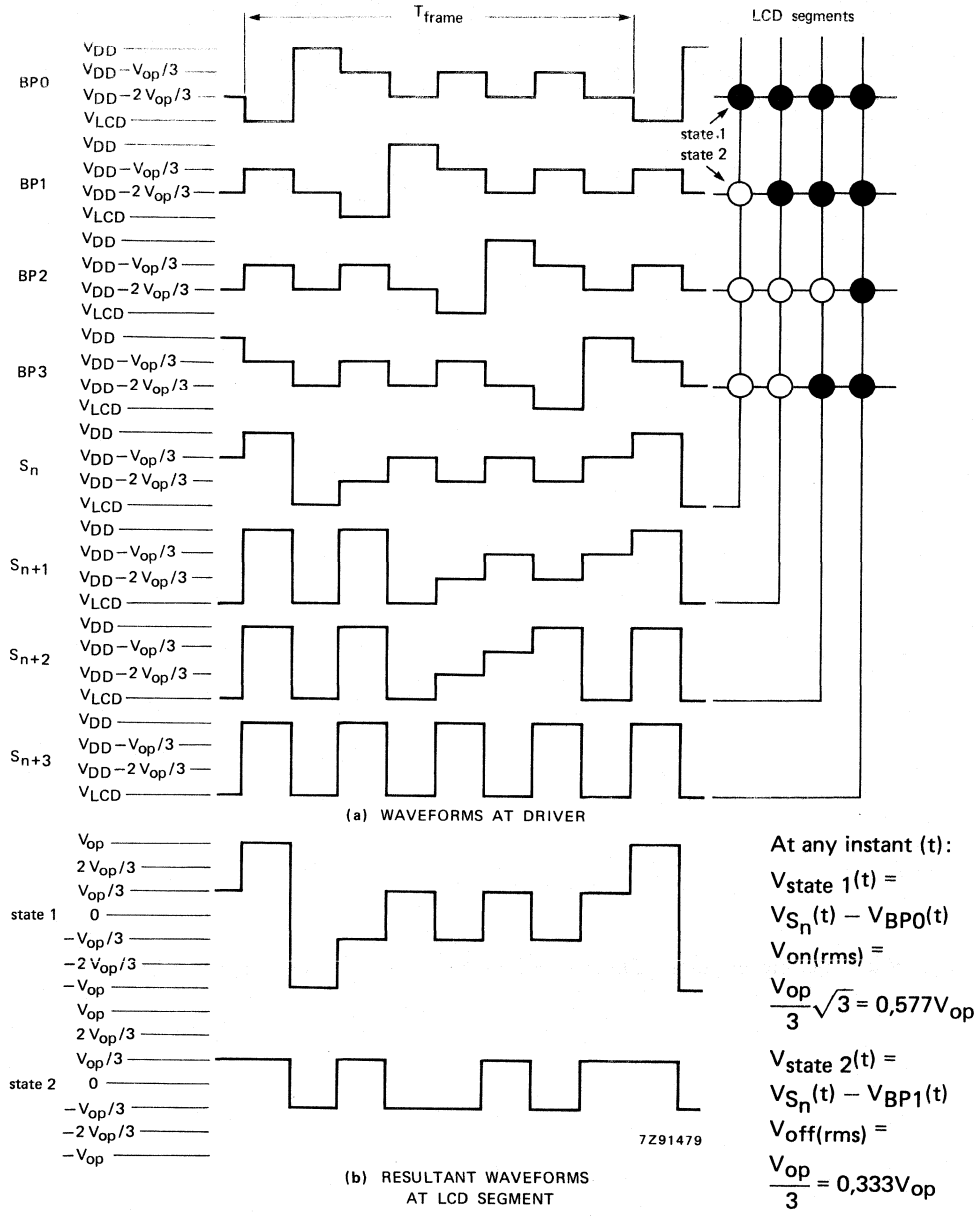


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

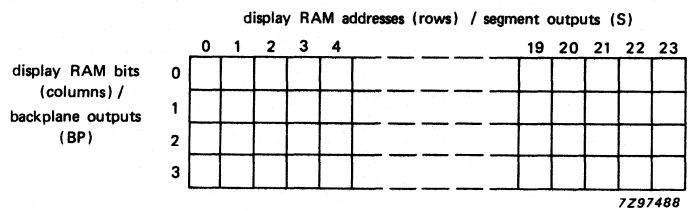


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

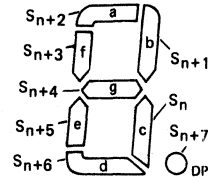
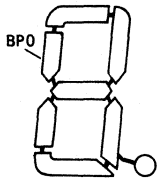
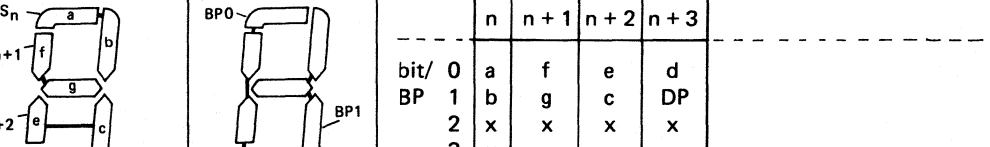
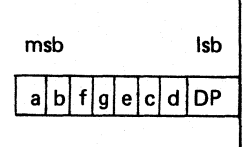
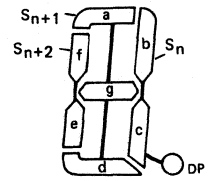
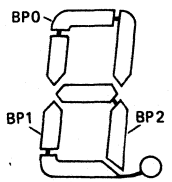
Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

<table>
<tr><th>drive mode</th><th>LCD segments</th><th>LCD backplanes</th><th>display RAM filling order</th><th>transmitted display byte</th></tr>
<tr><td>static</td><td> 
</td><td> 
</td><td> 
</td><td> 
</td></tr>
<tr><td>1 : 2
multiplex</td><td>
</td><td>
</td><td>
</td><td>
</td></tr>
<tr><td>1 : 3
multiplex</td><td> 
</td><td> 
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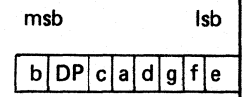
</td><td> 
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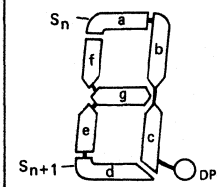
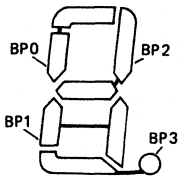
multiplex</td><td> 
</td><td> 
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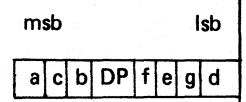
</td><td> 
</td></tr>
</table>

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

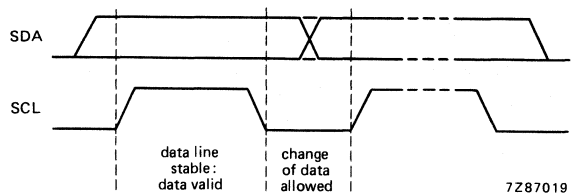


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

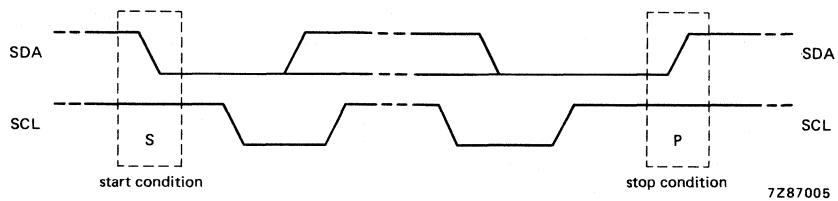


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

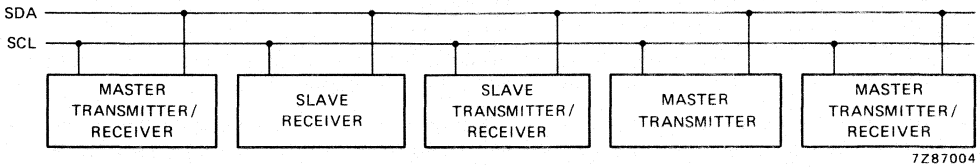


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

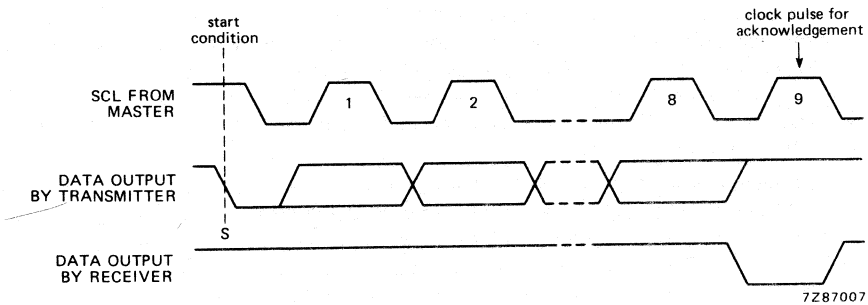


Fig. 14 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are available on request.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

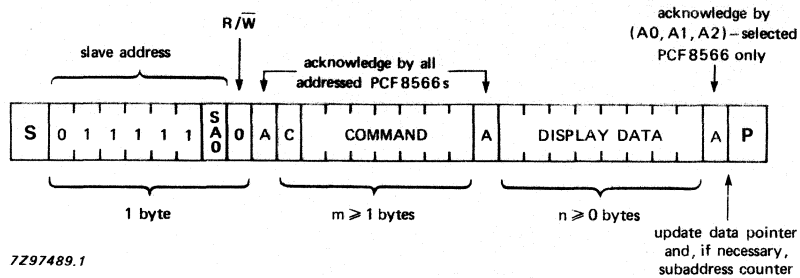


Fig. 15 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

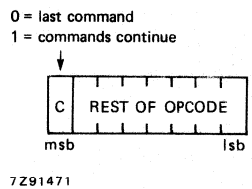


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

command/opcode	options	description
BANK SELECT C 1 1 1 1 0 I O	static / 1 : 2 MUX / bit I RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1 static / 1 : 2 MUX / bit O RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1	Defines input bank selection (storage of arriving display data) Defines output bank selection (retrieval of LCD display data) The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency / bits BF1 / BF0 off / 0 / 0 2 Hz / 0 / 1 1 Hz / 1 / 0 0,5 Hz / 1 / 1 blink mode / bit A normal blinking / 0 alternation blinking / 1	Defines the blinking frequency Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

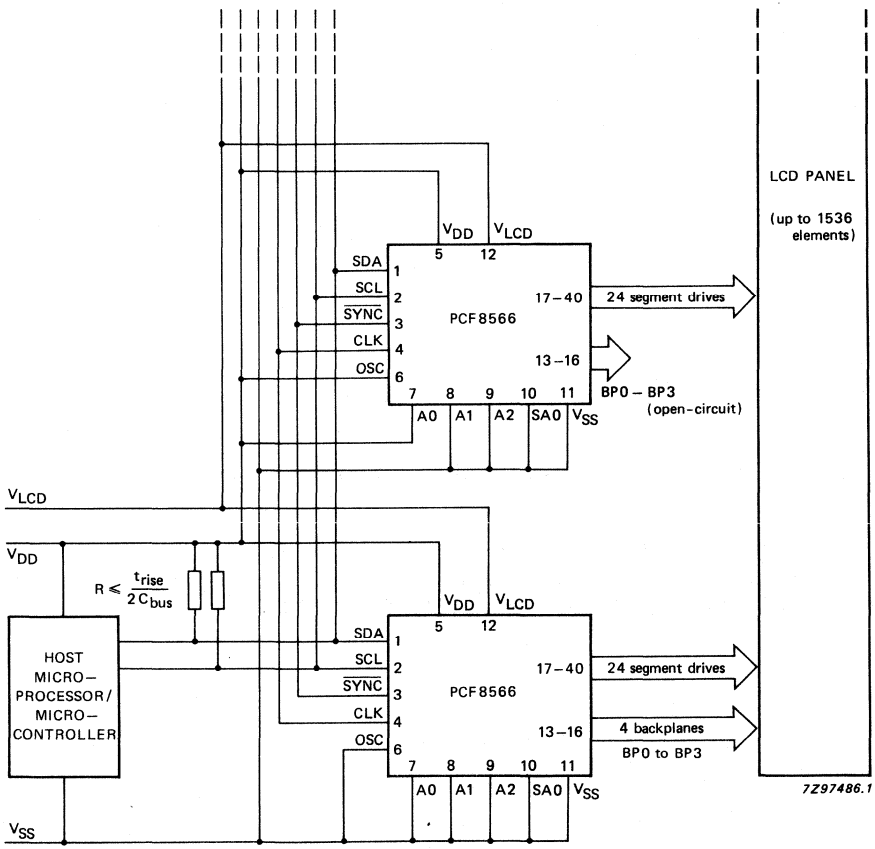


Fig. 17 Cascaded PCF8566 configuration.

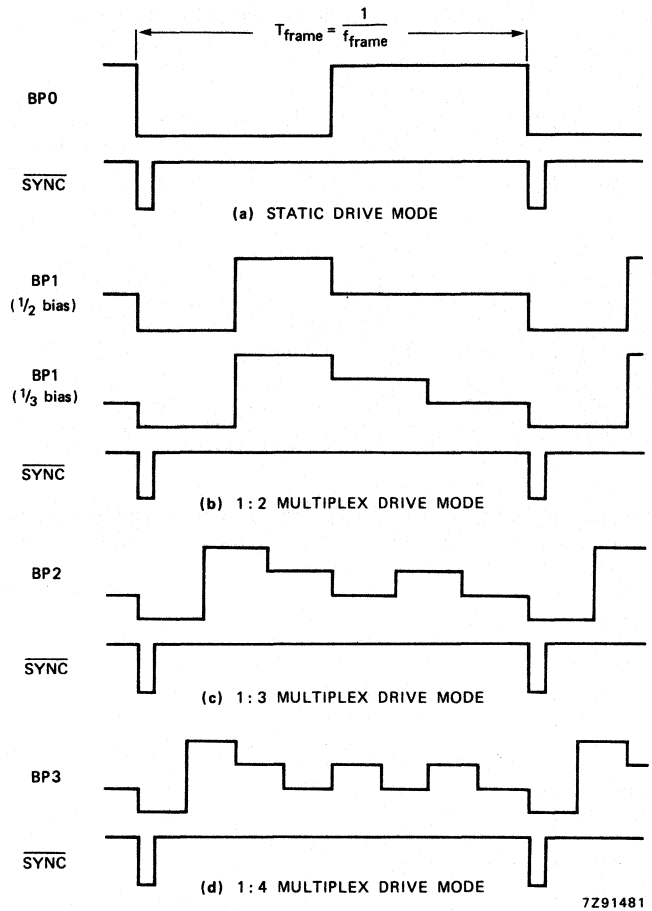


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD} - 5$ V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD} - 5$ V (note 4)	R_S	–	3	7,0	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{\text{SYNC}}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{\text{SYNC}}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

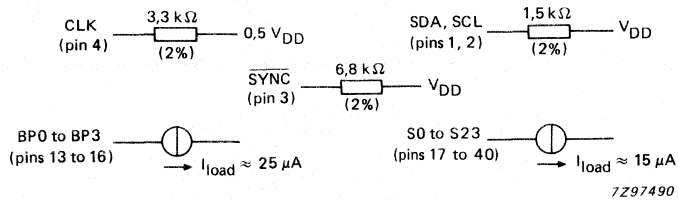


Fig. 19 Test loads.

DEVELOPMENT DATA

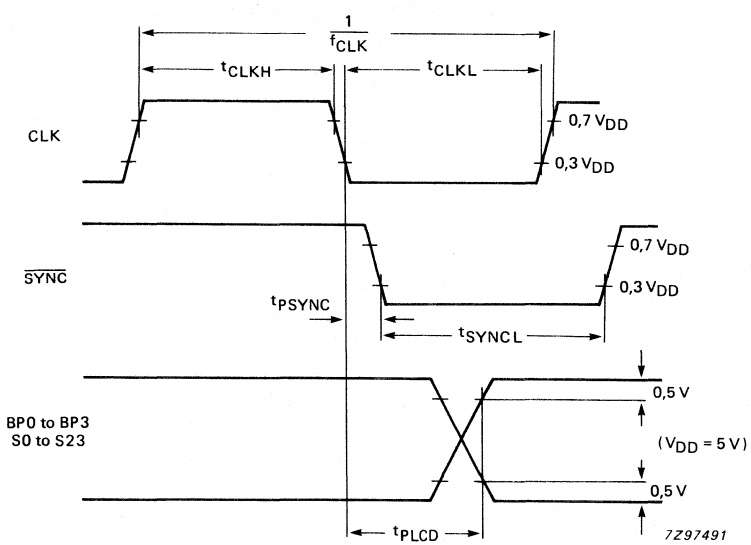


Fig. 20 Driver timing waveforms.

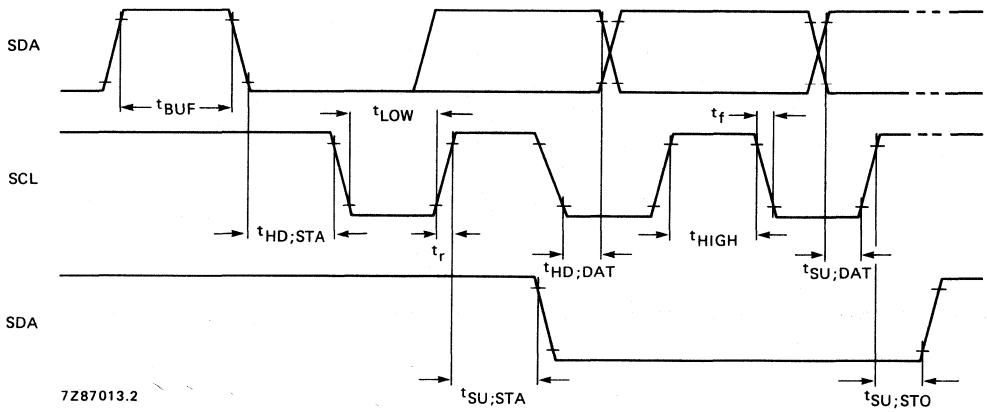
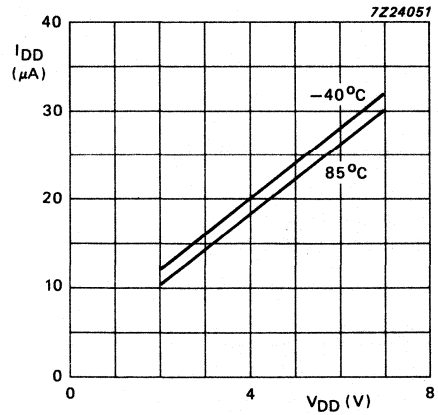
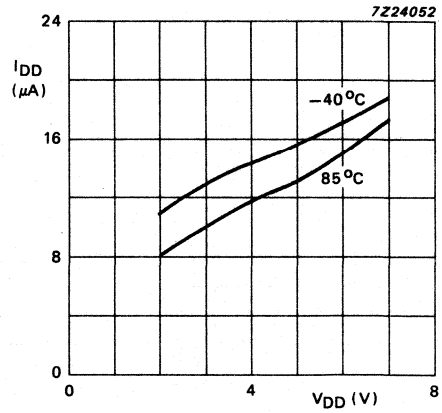


Fig. 21 I^2C bus timing waveforms.



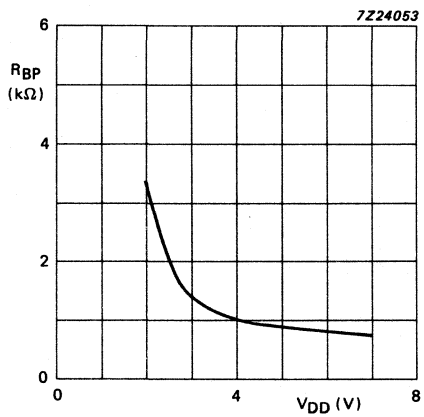
(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.



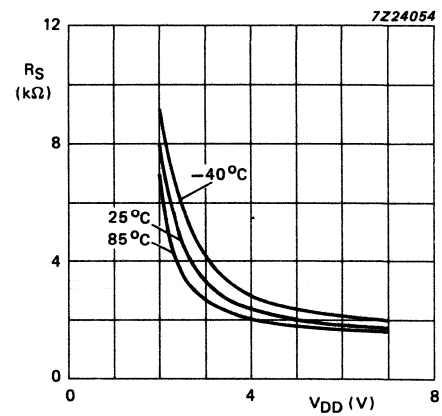
(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

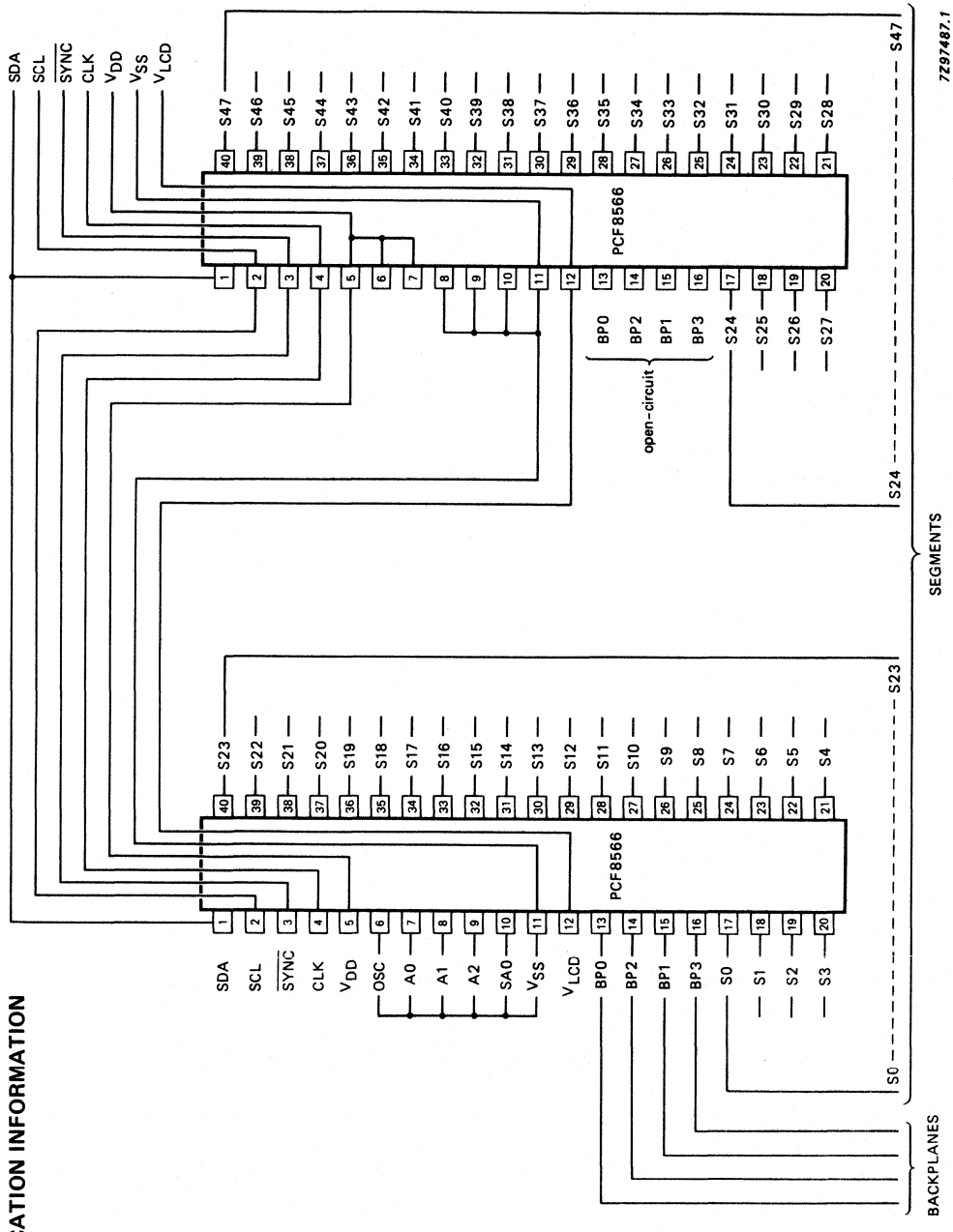


Fig. 24 Single plane wiring of packaged PCF8566s.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24 segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

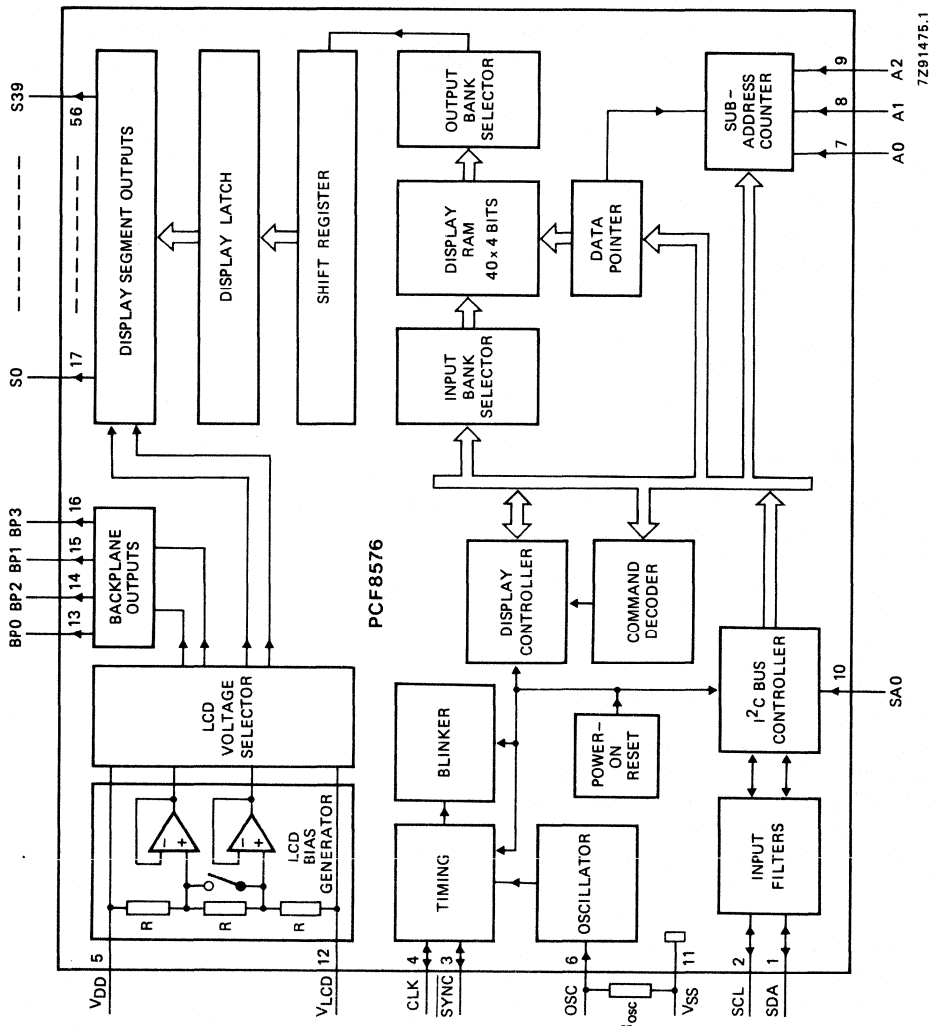


Fig. 1 Block diagram.

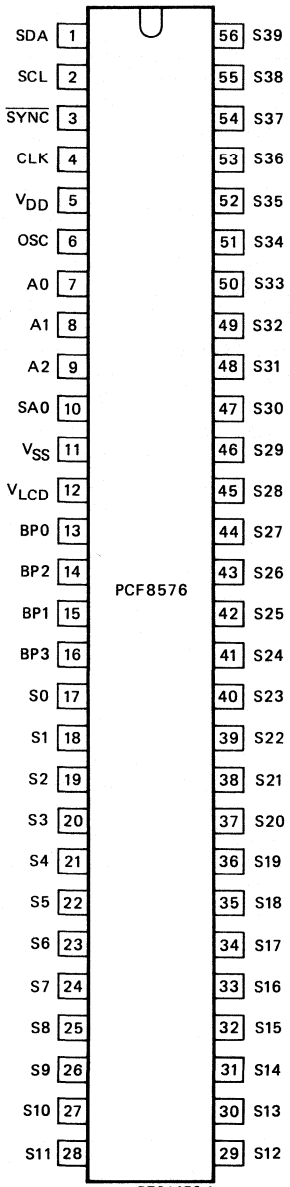


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropiate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

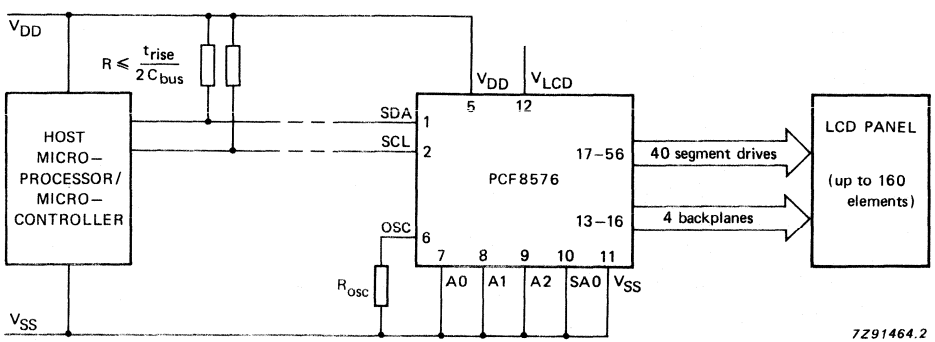


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\;V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

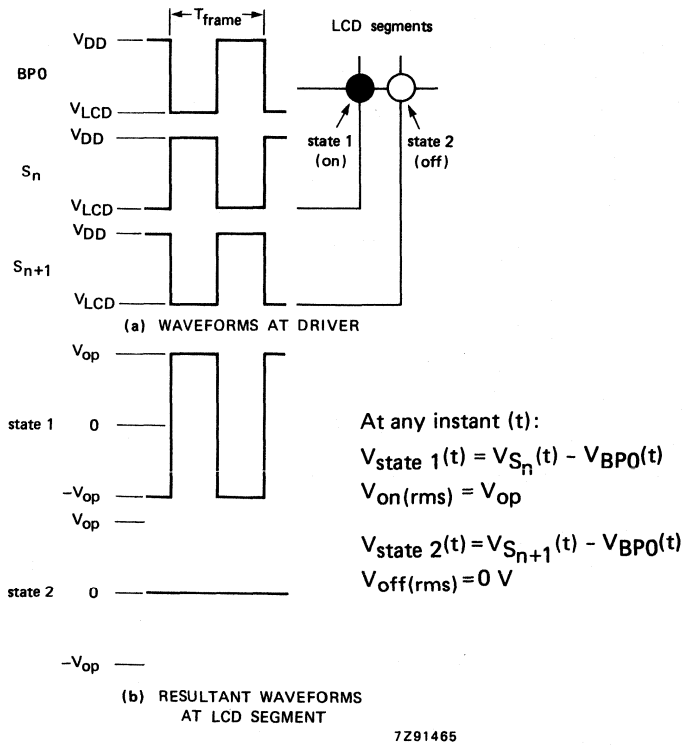


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

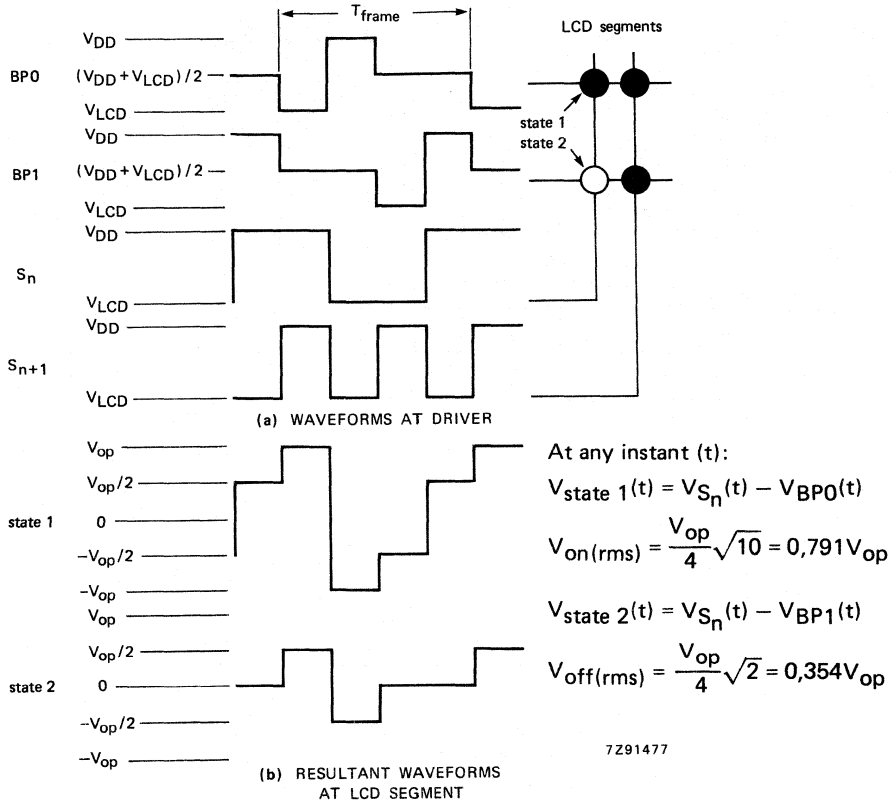


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

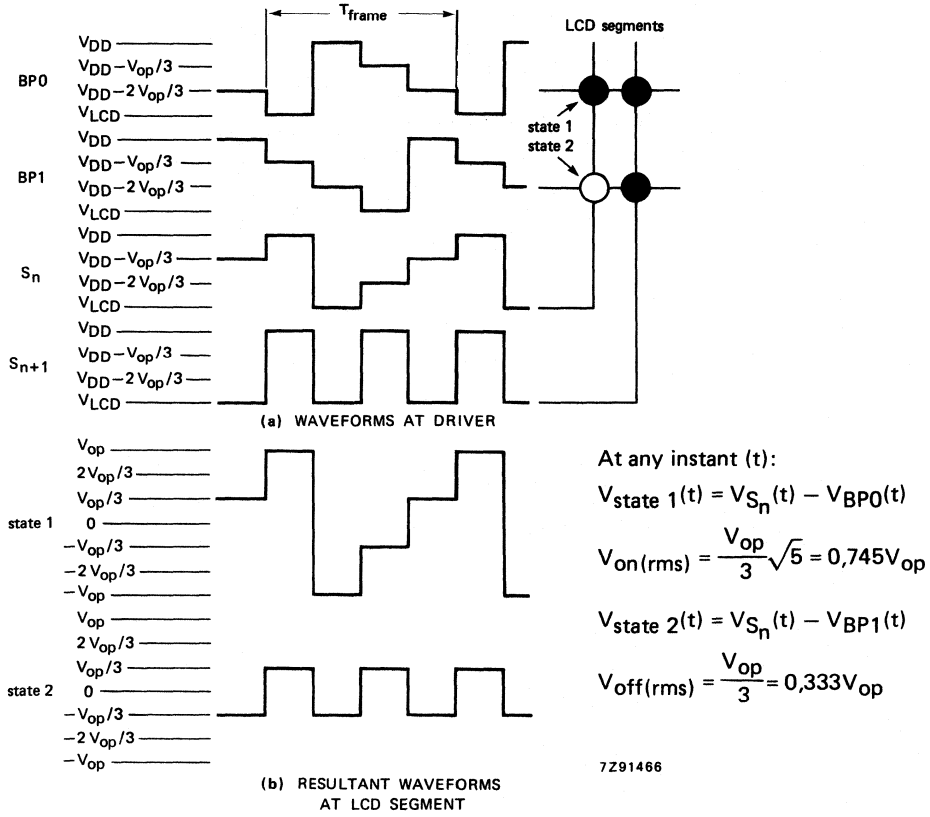


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

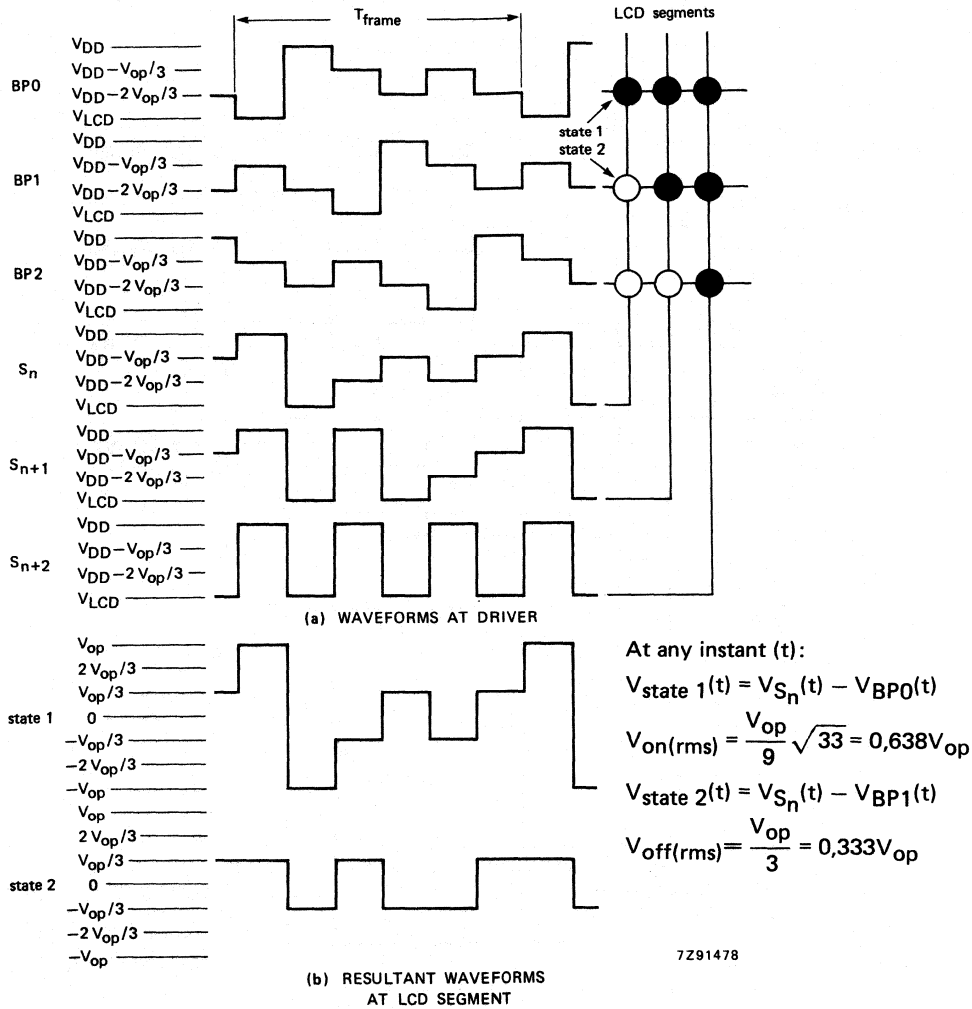


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

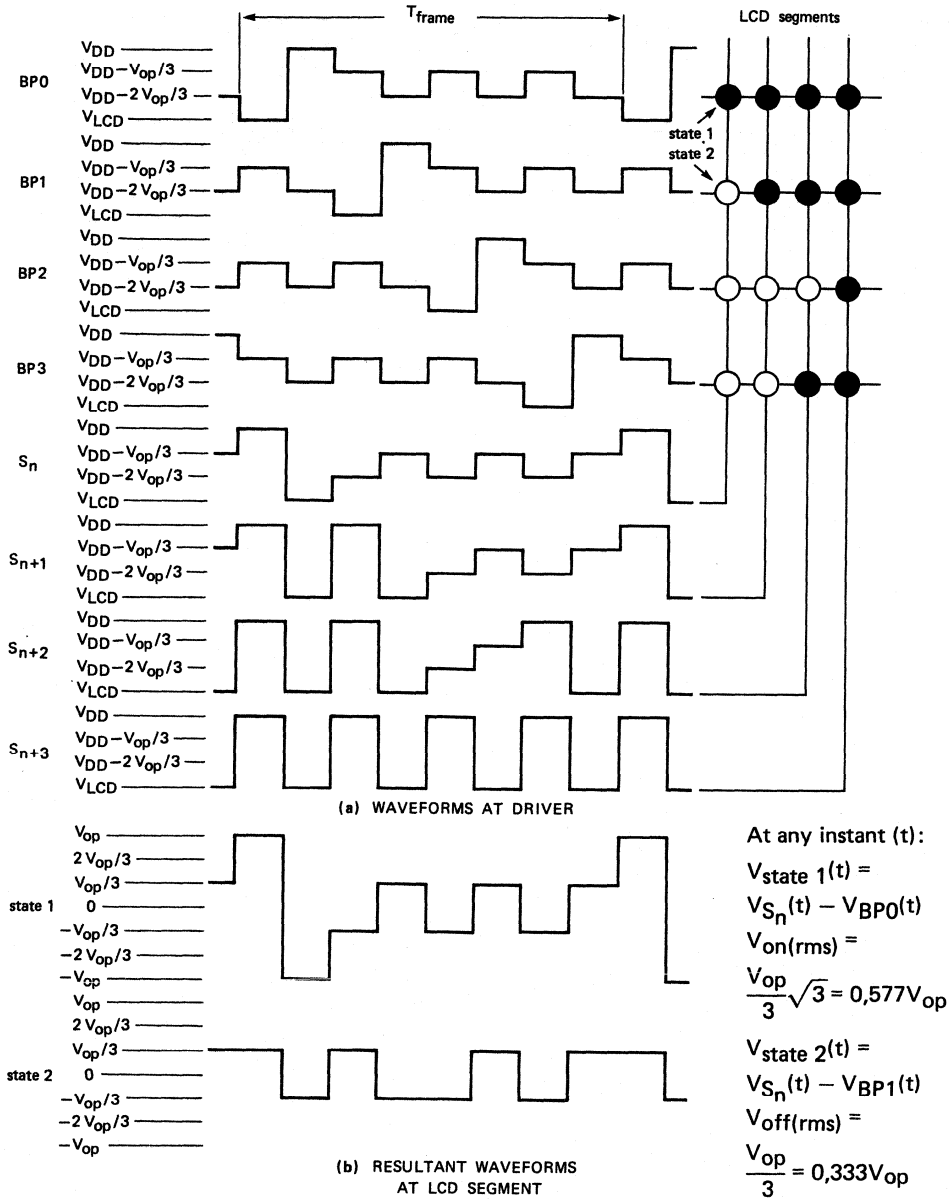


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

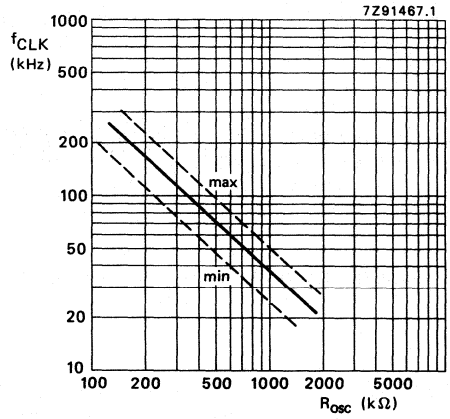


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7/R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{osc} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{osc} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{osc} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

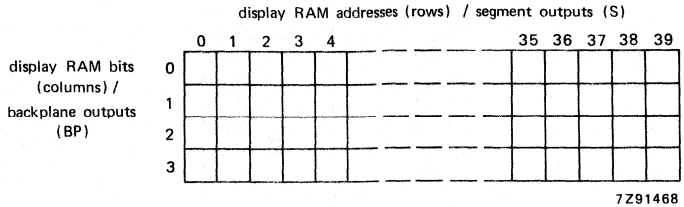


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

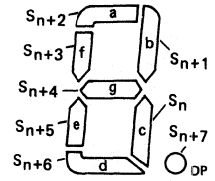
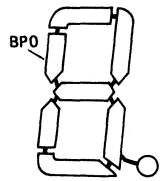
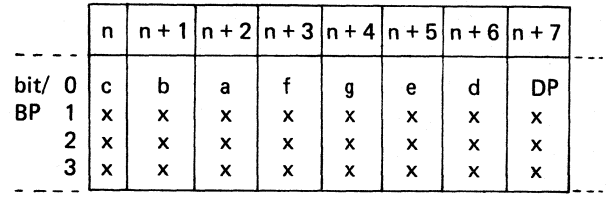
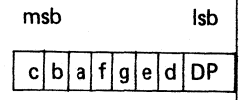
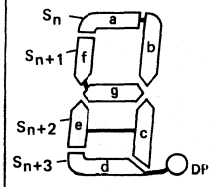
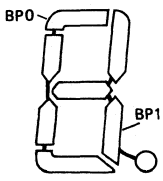
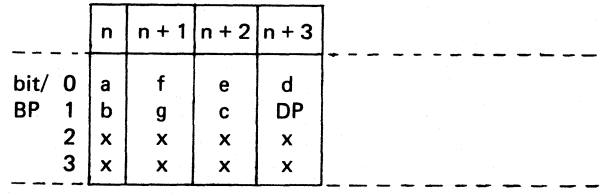
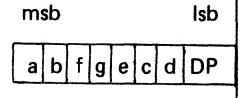
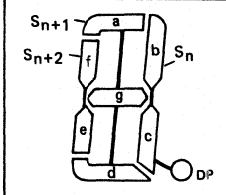
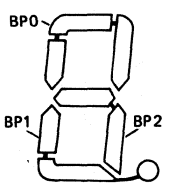
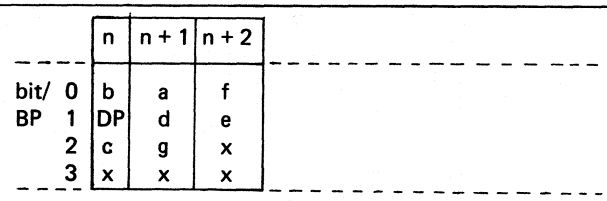
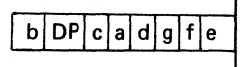
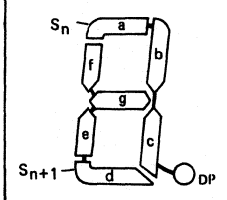
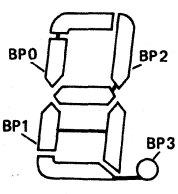
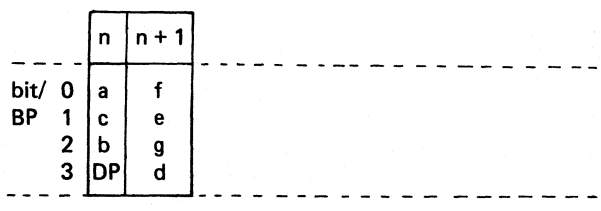
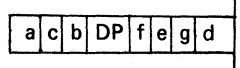
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

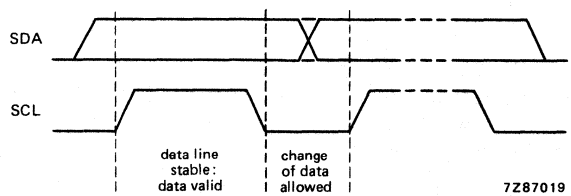


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

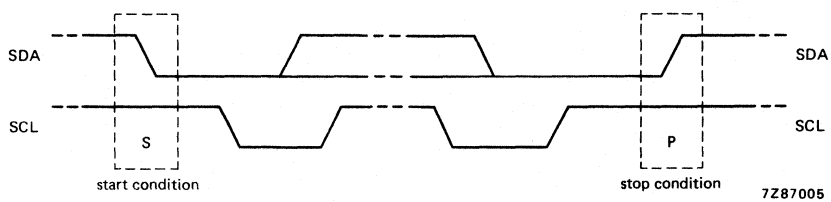


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

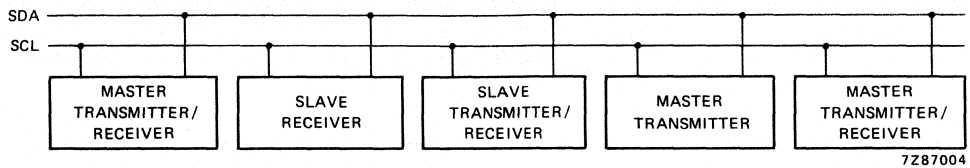


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

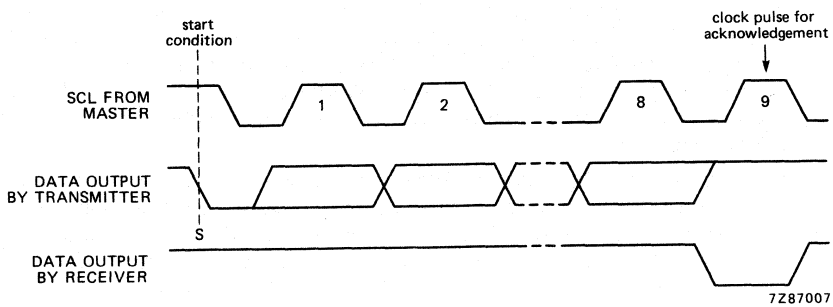


Fig. 15 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

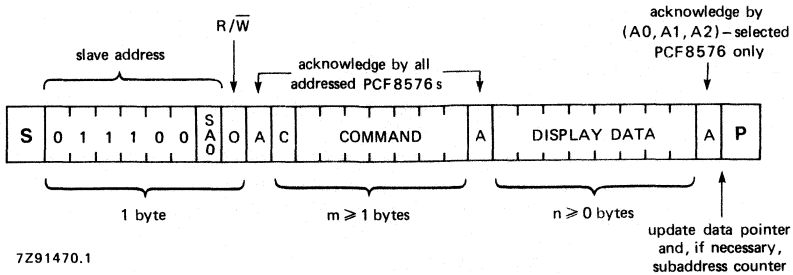


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

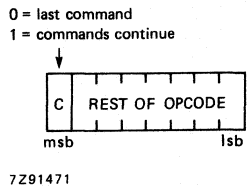


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C | 1 1 1 1 0 | I | O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C | 1 1 1 0 | A | BF1 BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

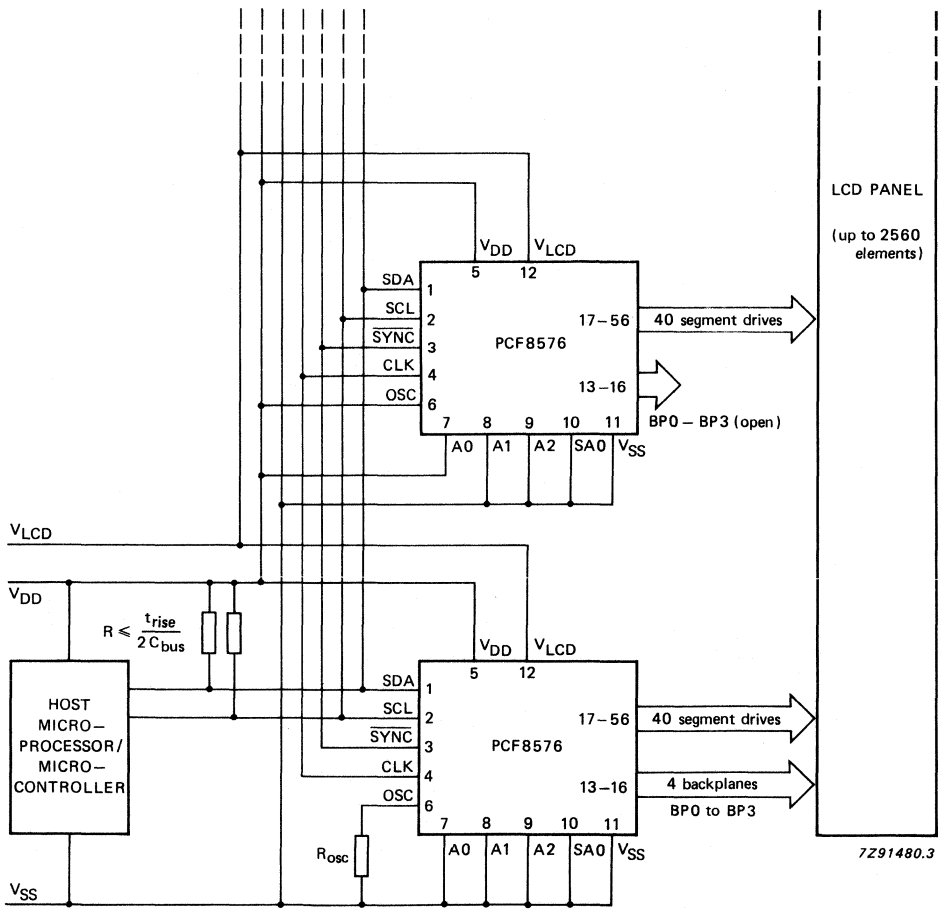
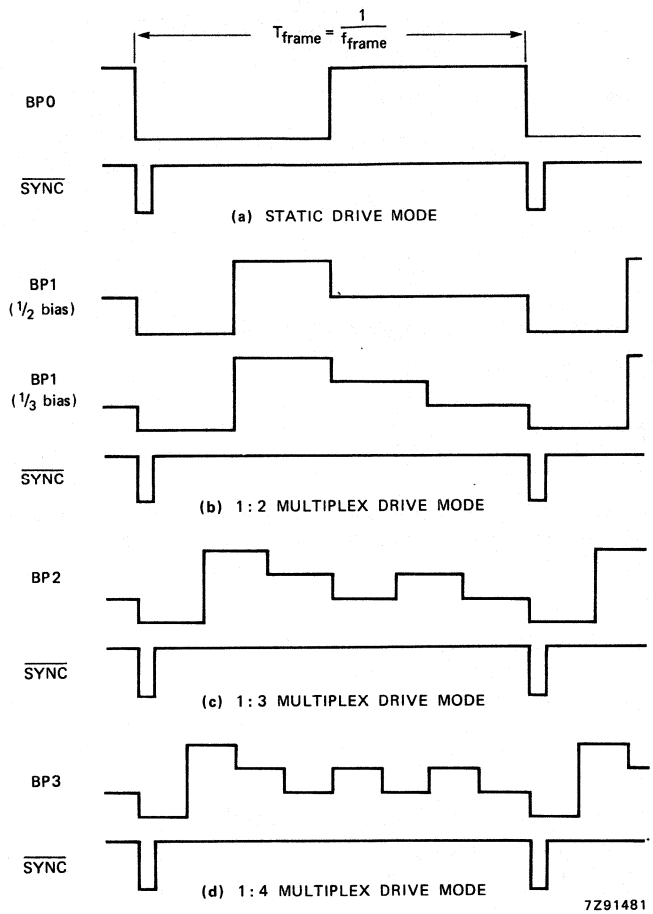


Fig. 18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;

T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;

$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

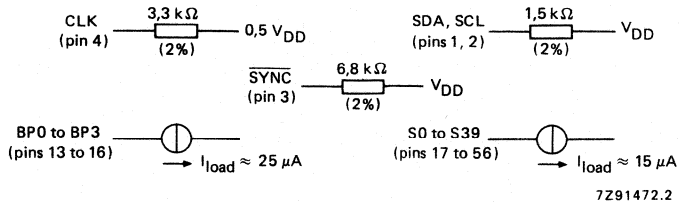


Fig. 20 Test loads.

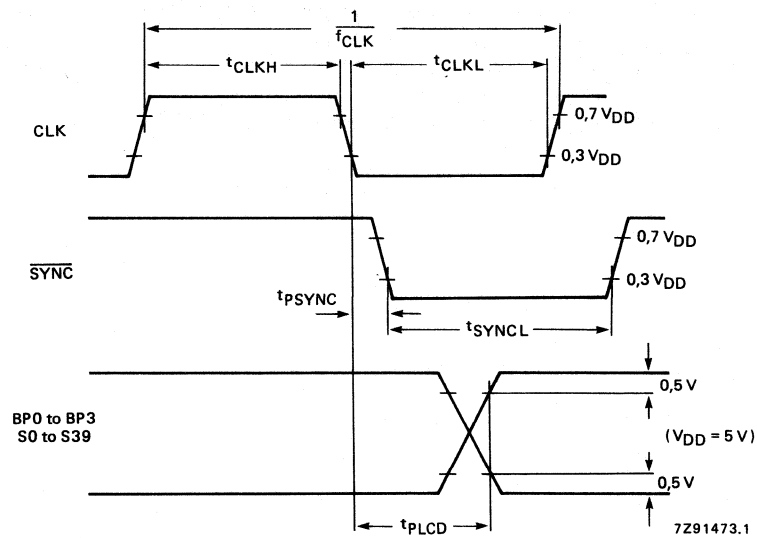


Fig. 21 Driver timing waveforms.

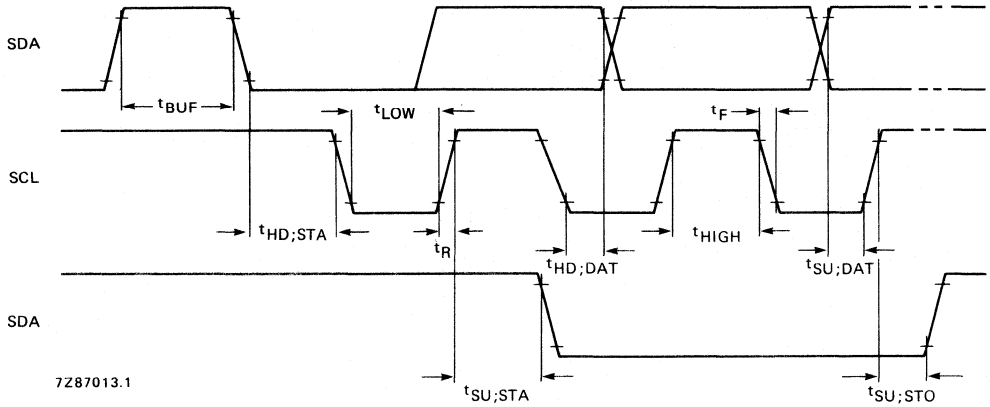
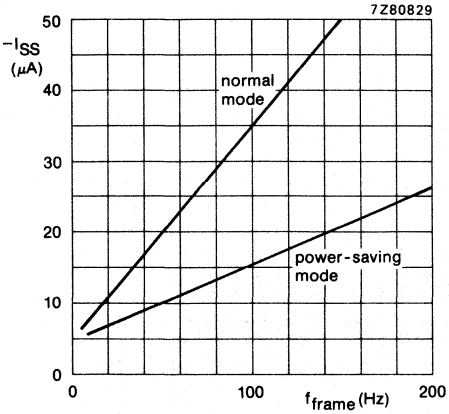
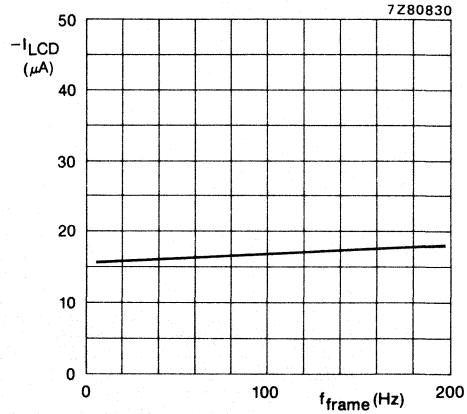


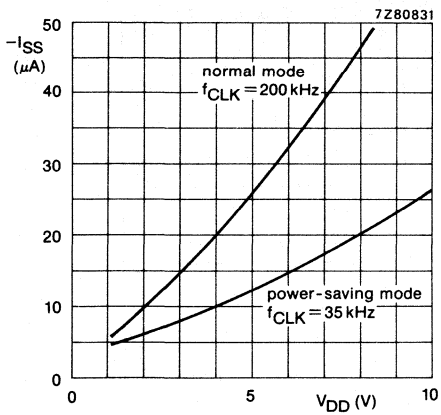
Fig. 22 I²C bus timing waveforms.



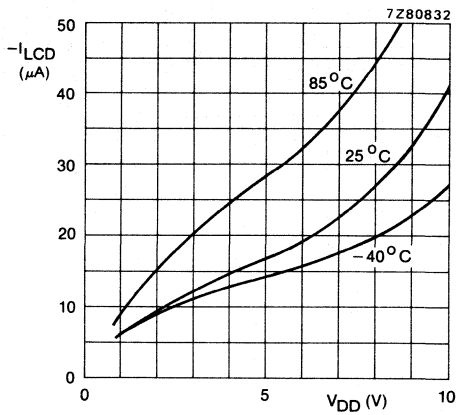
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

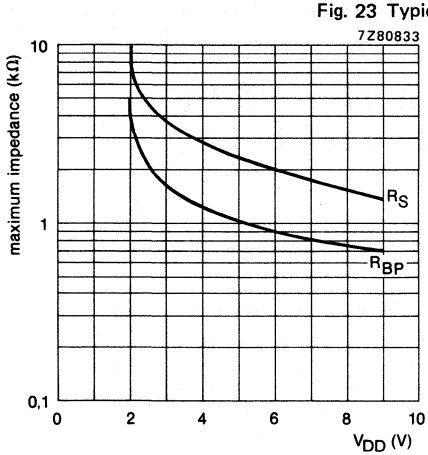


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

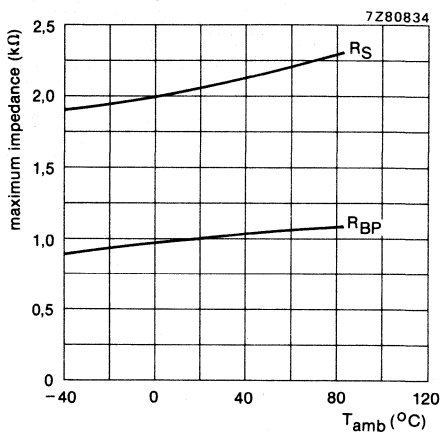


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

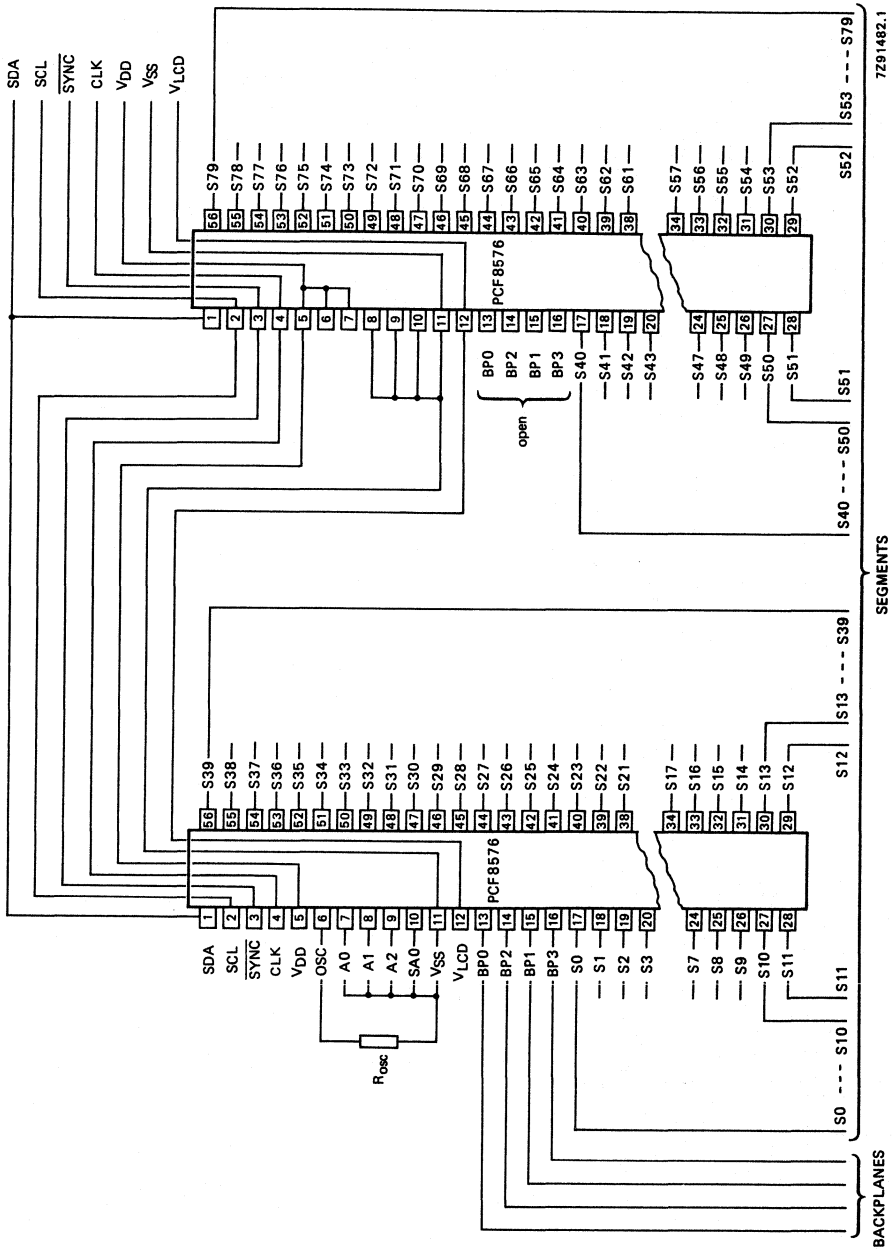


Fig. 25 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

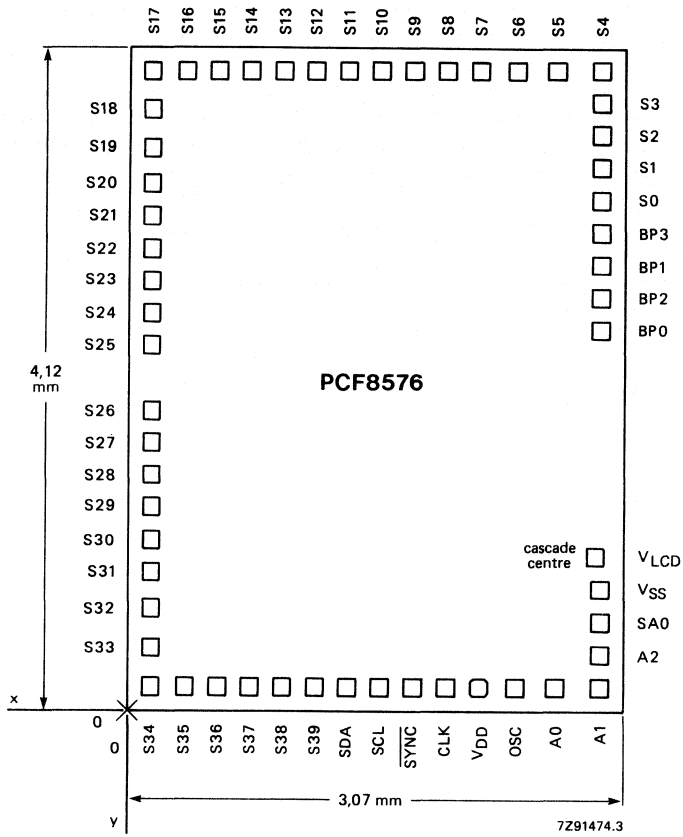


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380	↑	↑
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640	↓	↓
A1	2910	160	bottom
S17	160	3960	top
S16	380	↑	↑
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32	↑	640	↑
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19	↓	3480	
S18	160	3720	left
A2	2910	360	right
SA0	↕	560	↑
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2	↑	2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

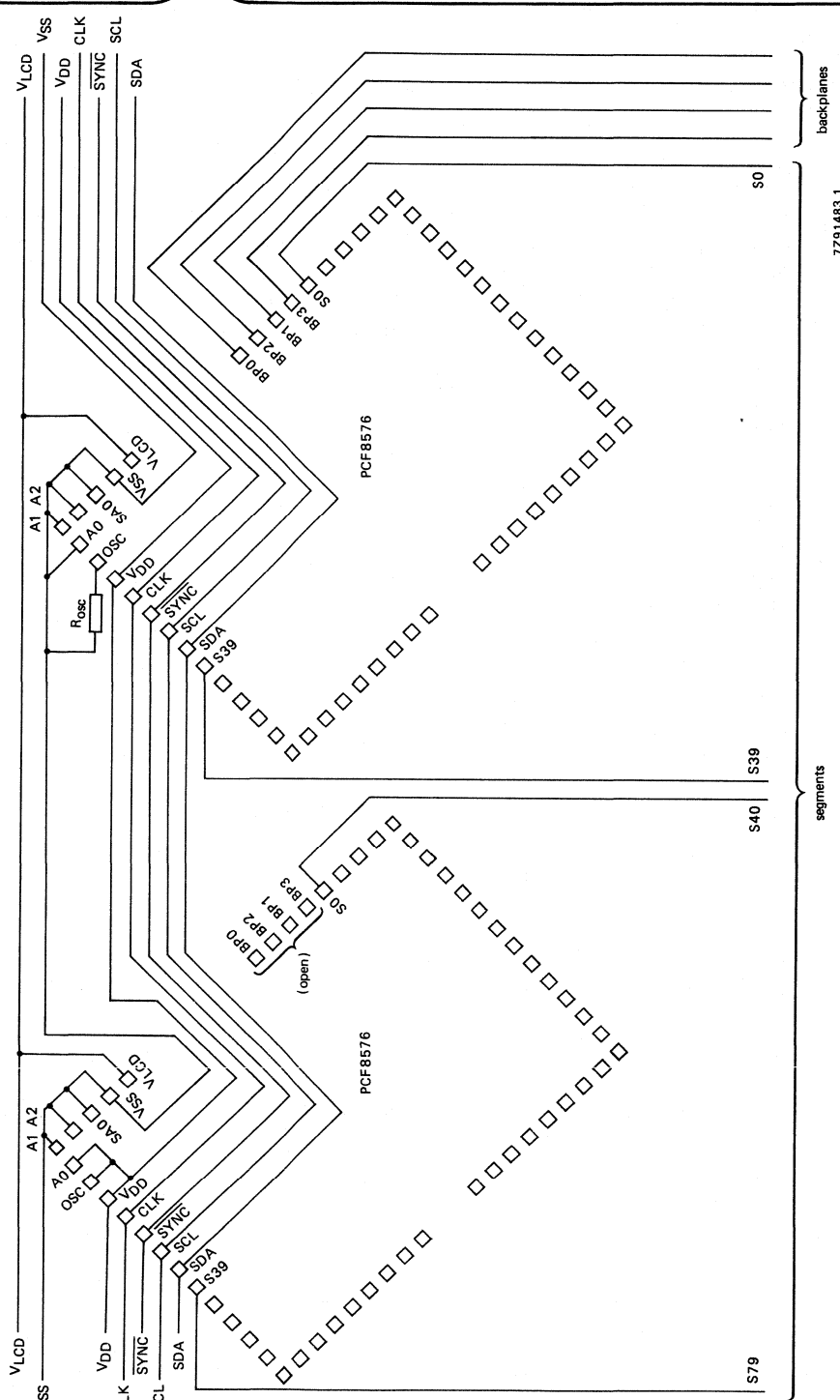


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

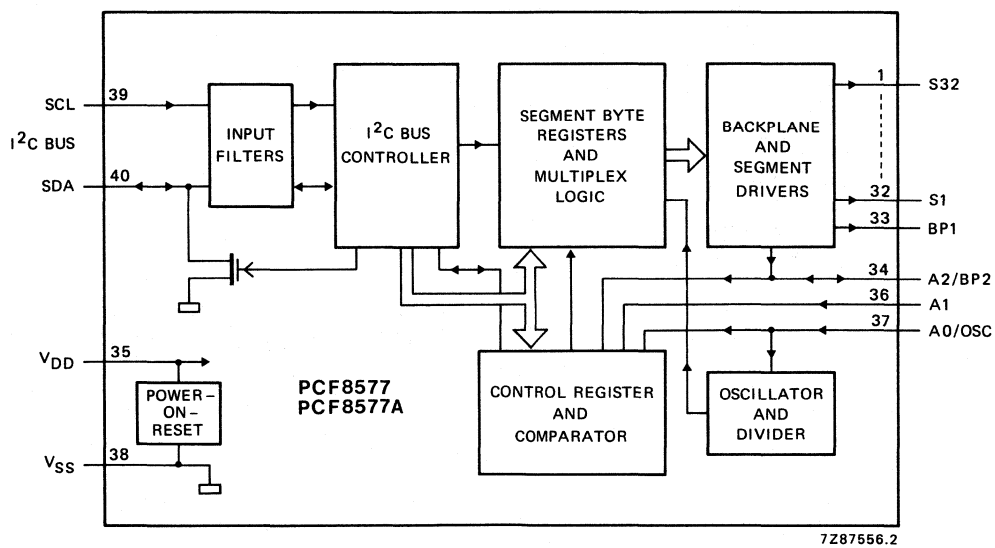


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT-129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

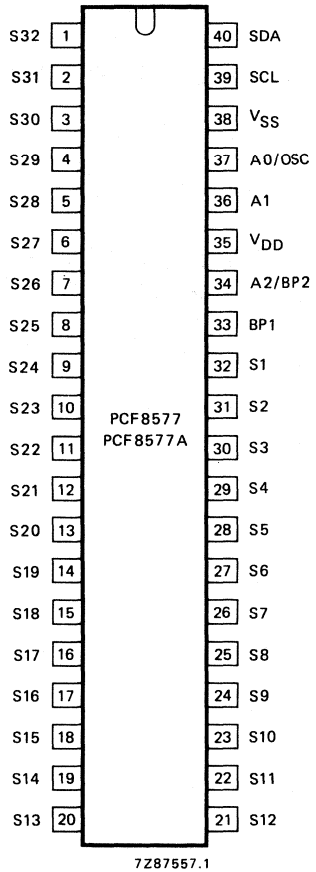


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

DEVELOPMENT DATA

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

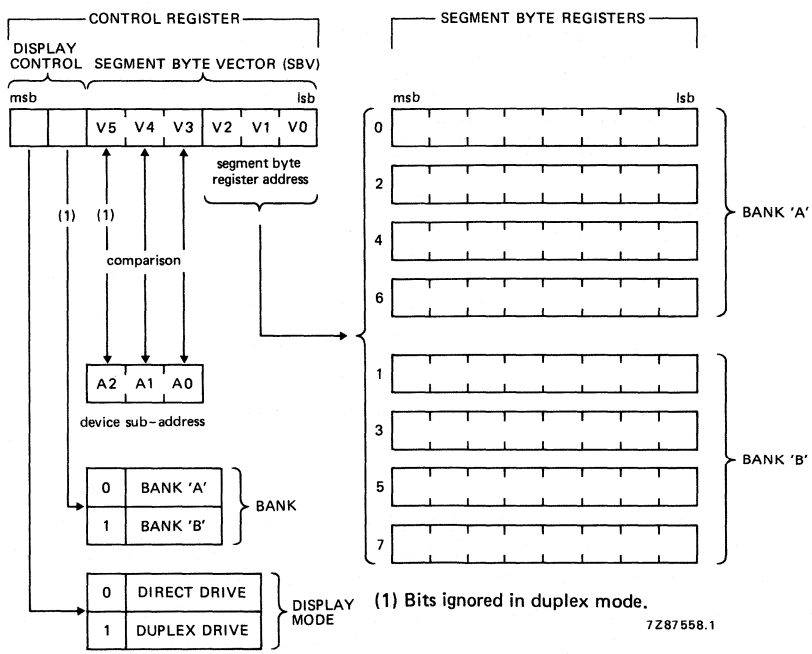


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

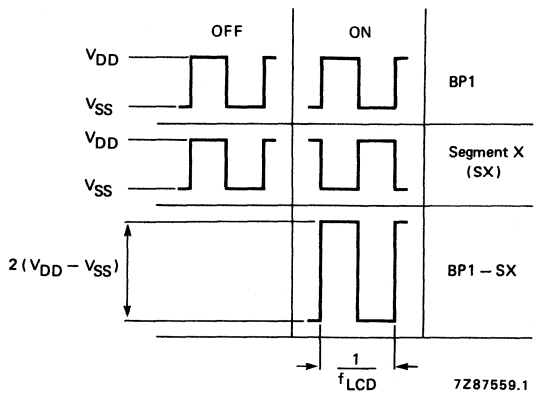
After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.



$V_{ON} = V_{DD} - V_{SS}$
$V_{OFF} = 0$

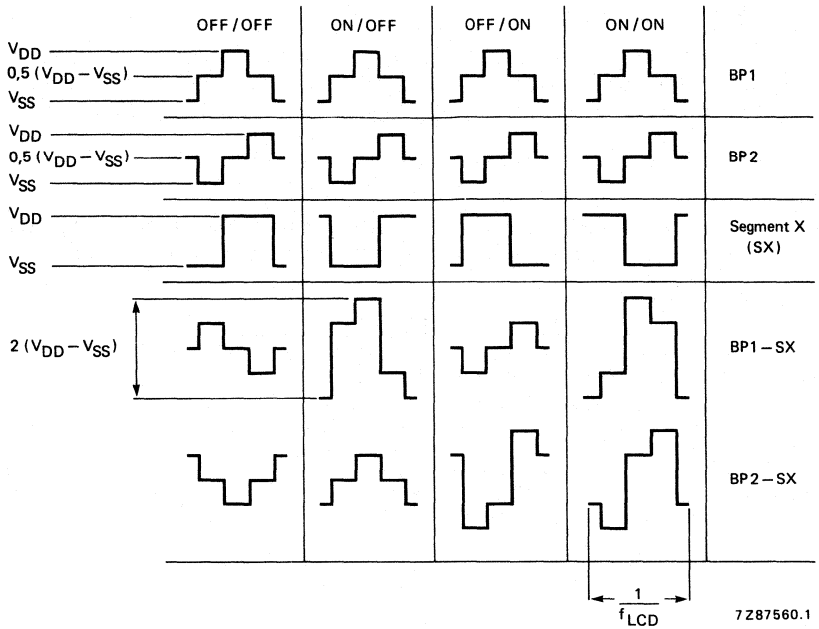
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2{,}26$

Fig. 5 Duplex mode display output waveforms.

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

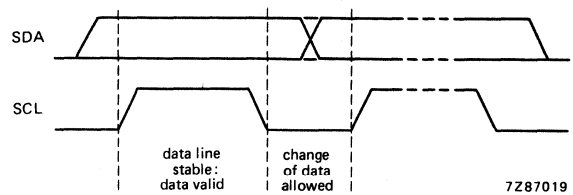


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

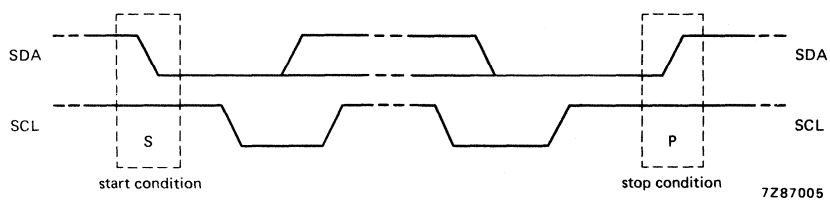


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

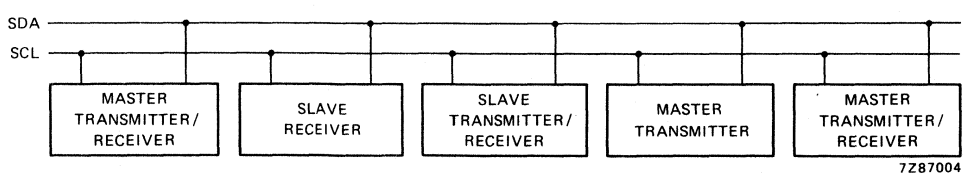


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

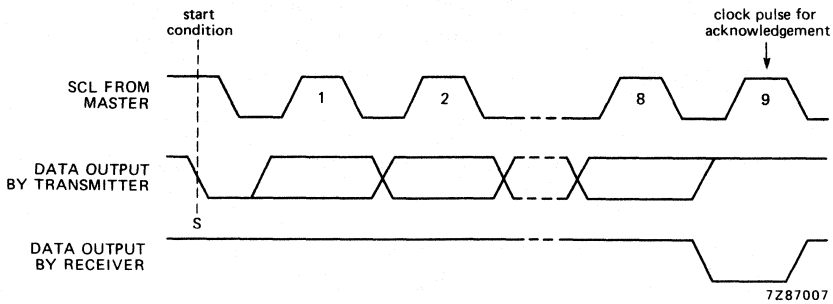


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

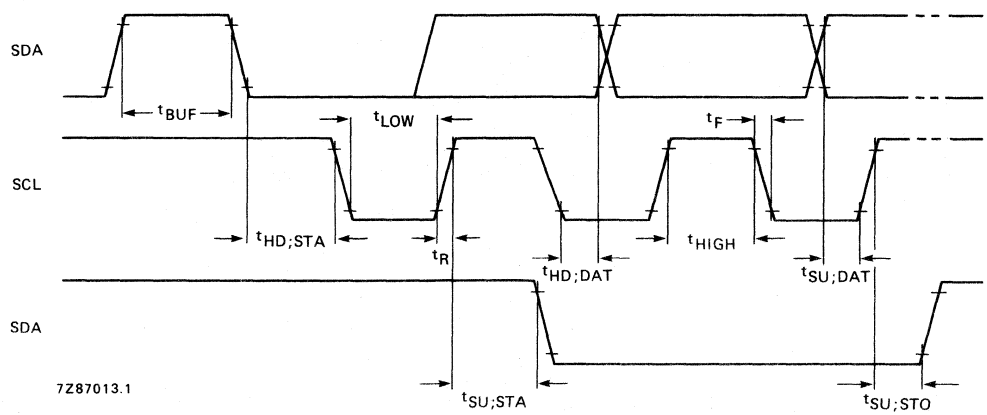


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

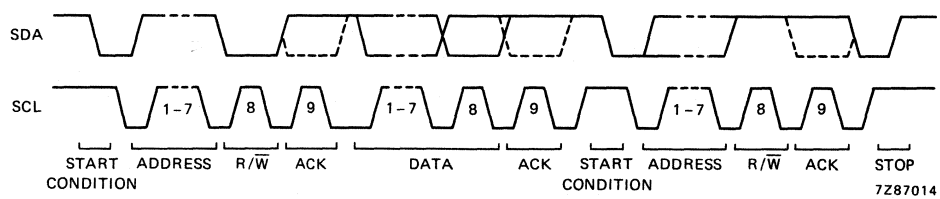


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

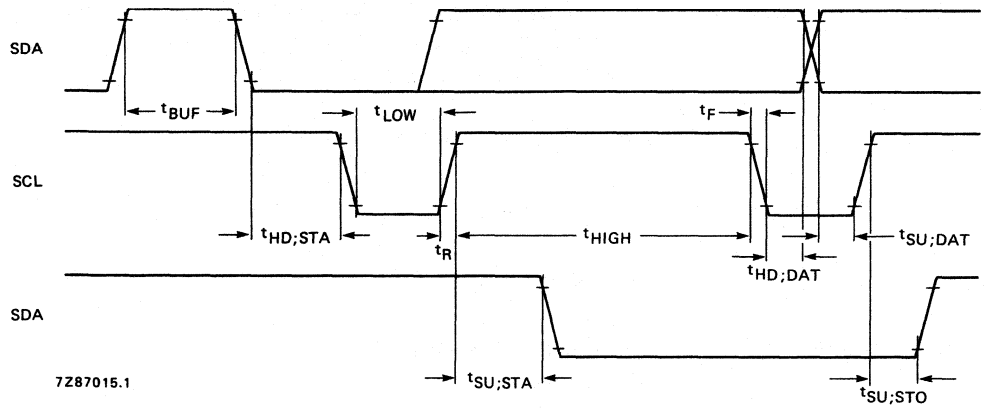


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS (continued)

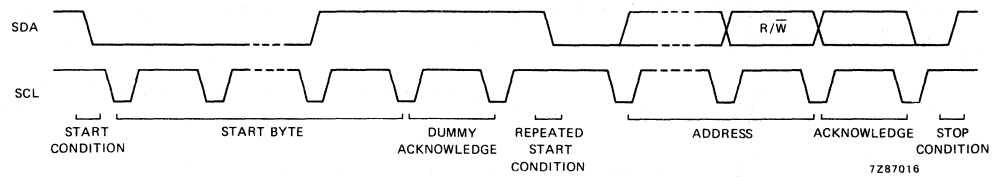


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

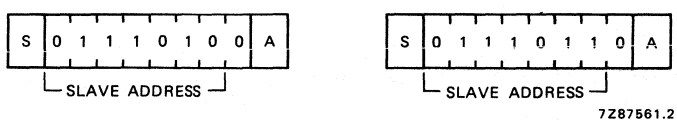
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577. (b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

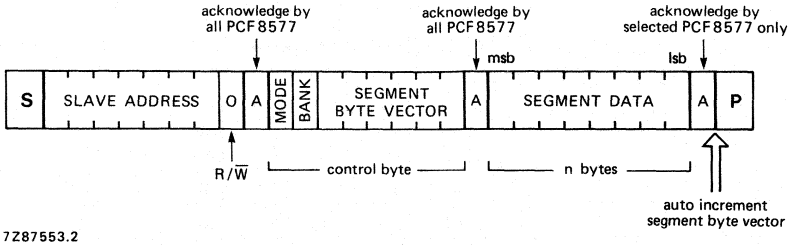


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

DEVELOPMENT DATA

CHARACTERISTICS

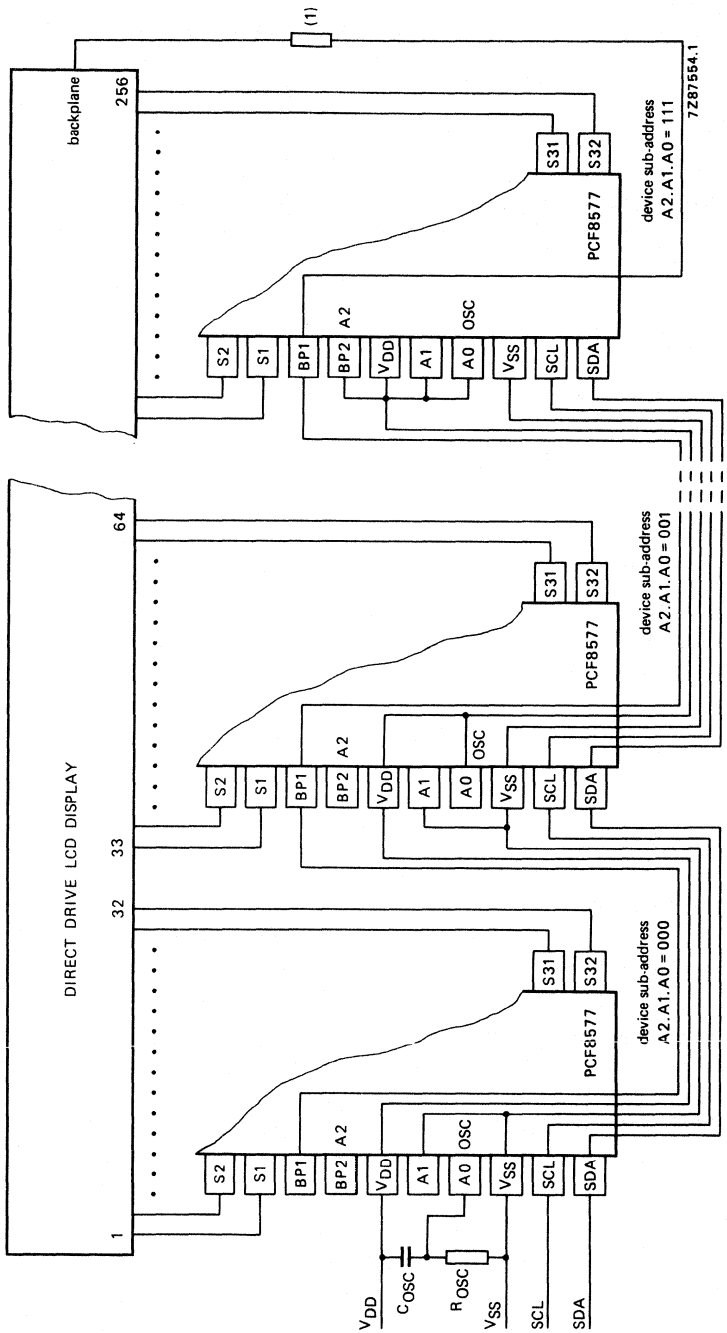
V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	70	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at V_I = V_{SS}	C_I	–	–	7	pF
A1 input leakage current at V_I = V_{SS} or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at V_I = V_{DD}	I_I	–	2,0	–	μA
A0/OSC input current at V_I = V_{SS} or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current					
at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current					
at V_{OH} = V_{DD} − 0,4 V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times (V_{BP} − V_{SX})					
at maximum load	t_r, t_f	–	–	200	μs
Display frequency					
at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

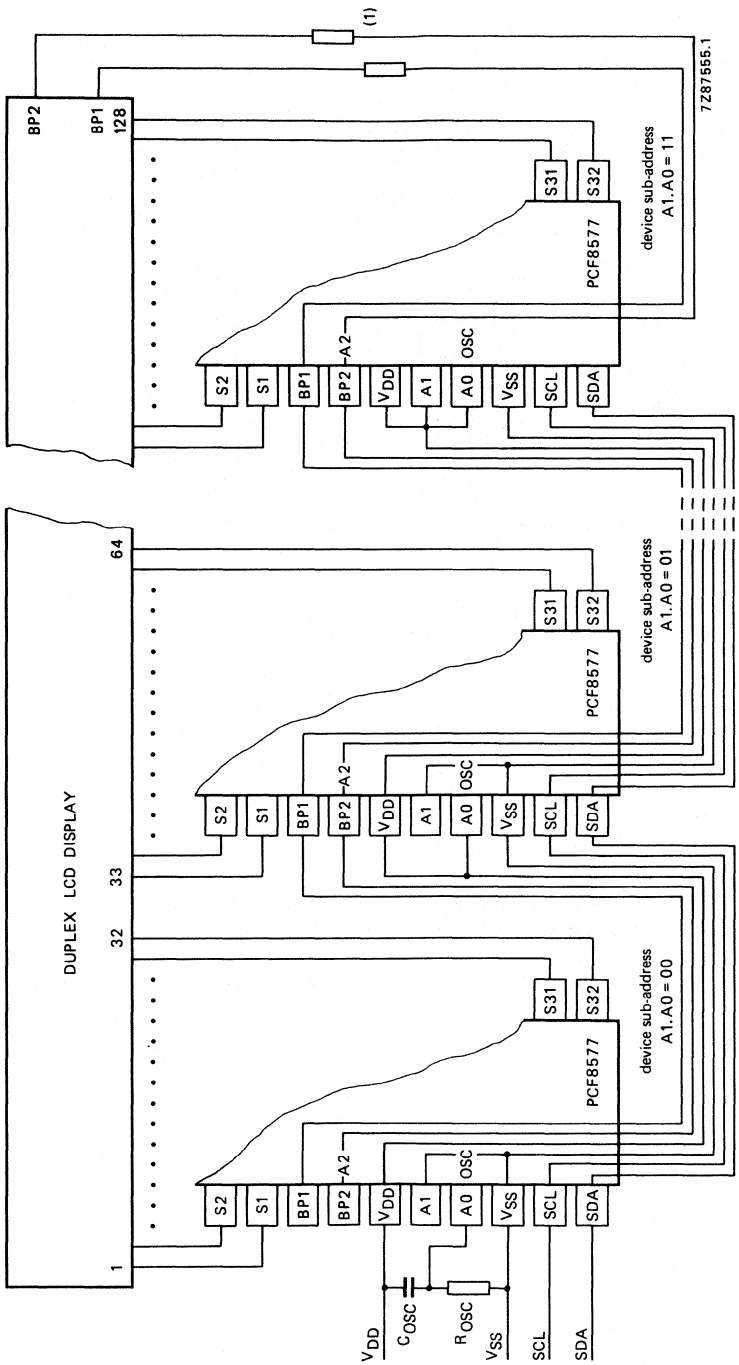
APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 Ω.

Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.

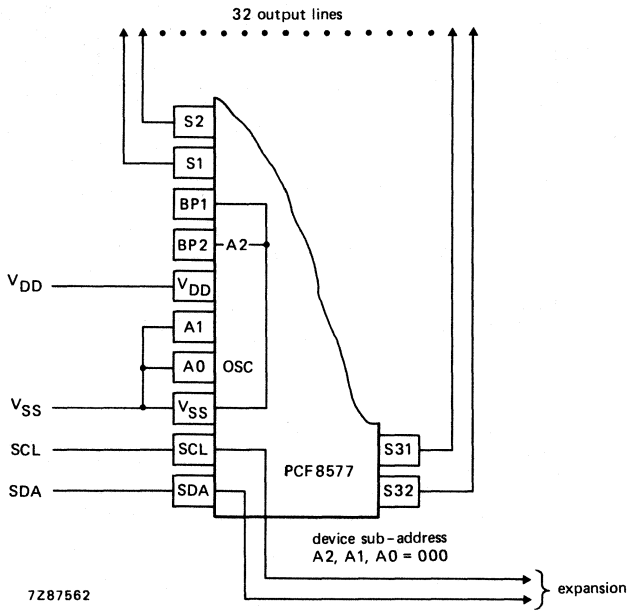
DEVELOPMENT DATA



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I^2C bus application.

LCD FLAT-PANEL ROW/COLUMN DRIVER

GENERAL DESCRIPTION

The PCF2201 is a row or column LCD driver, designed to drive LCD flat-panels at multiplex rates of up to 1 : 256. The PCF2201 converts serial or parallel 4-bit display data into parallel LCD drive waveforms, capable of driving up to 81 rows or 80 columns of an LCD matrix. The PCF2201 is cascadable, enabling it to drive any LCD flat-panel matrix. The PCF2201 is controlled by an alphanumeric/graphic controller.

Features

- Row or column drive capability
- 80 data latches
- 81 stage bidirectional shift register
- 81 LCD drive outputs
- Proprietary margin control drive output
- Low drive impedance
- LCD drive voltage of up to 25 V
- 5 V logic compatibility
- High speed operation (4 MHz)
- Multiplex rates of up to 1 : 256
- Externally adjusted bias voltages
- Maximum LCD voltage and V_{DD} may be separated
- 64/65 pin programmable output operation mode
- Low power consumption
- Overall flat-panel power consumption minimized
- Pin programmable right/left orientation for convenience of flat-panel construction
- Optimized pinning for single plane wiring
- Space-saving 120-lead Tape-Automated Bonding package
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF2201V: 120-lead Tape-Automated Bonding package.

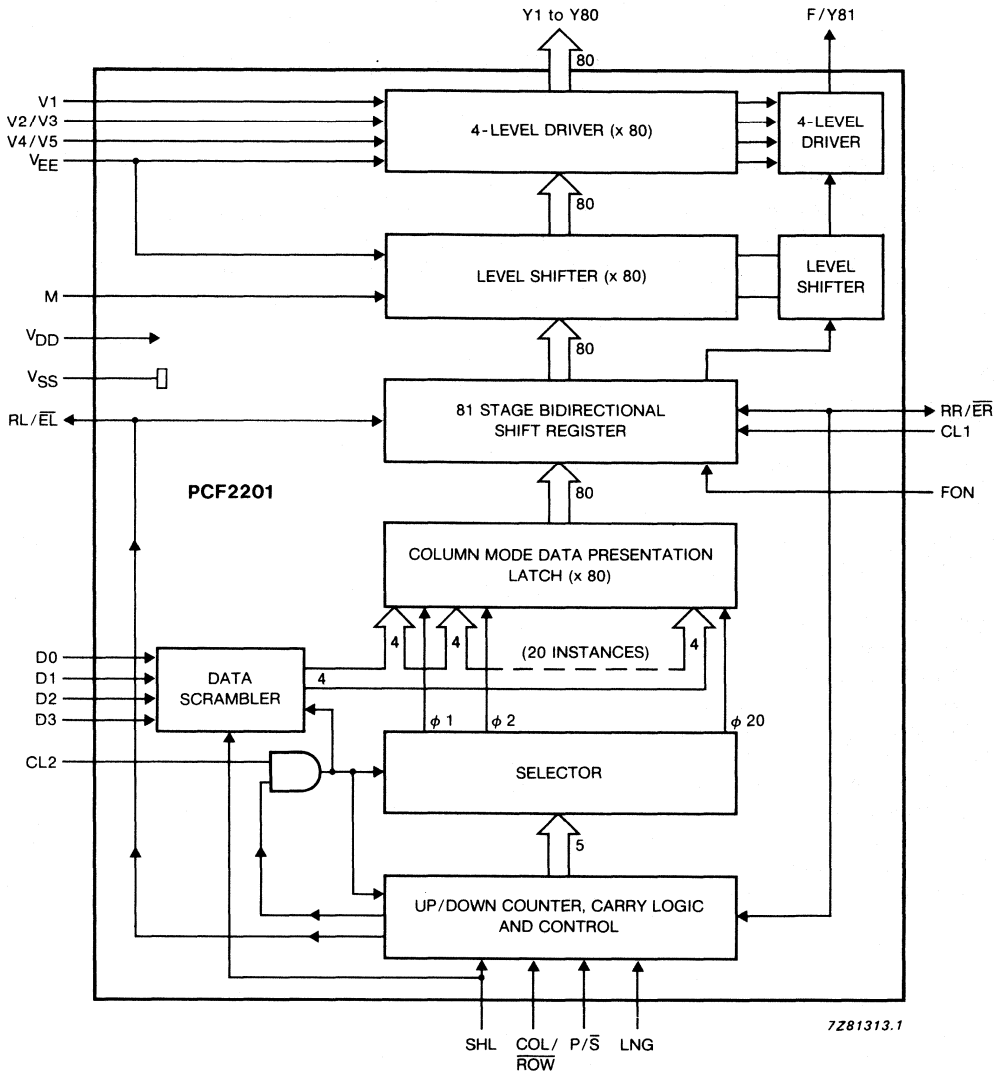


Fig. 1 Block diagram.

DEVELOPMENT DATA

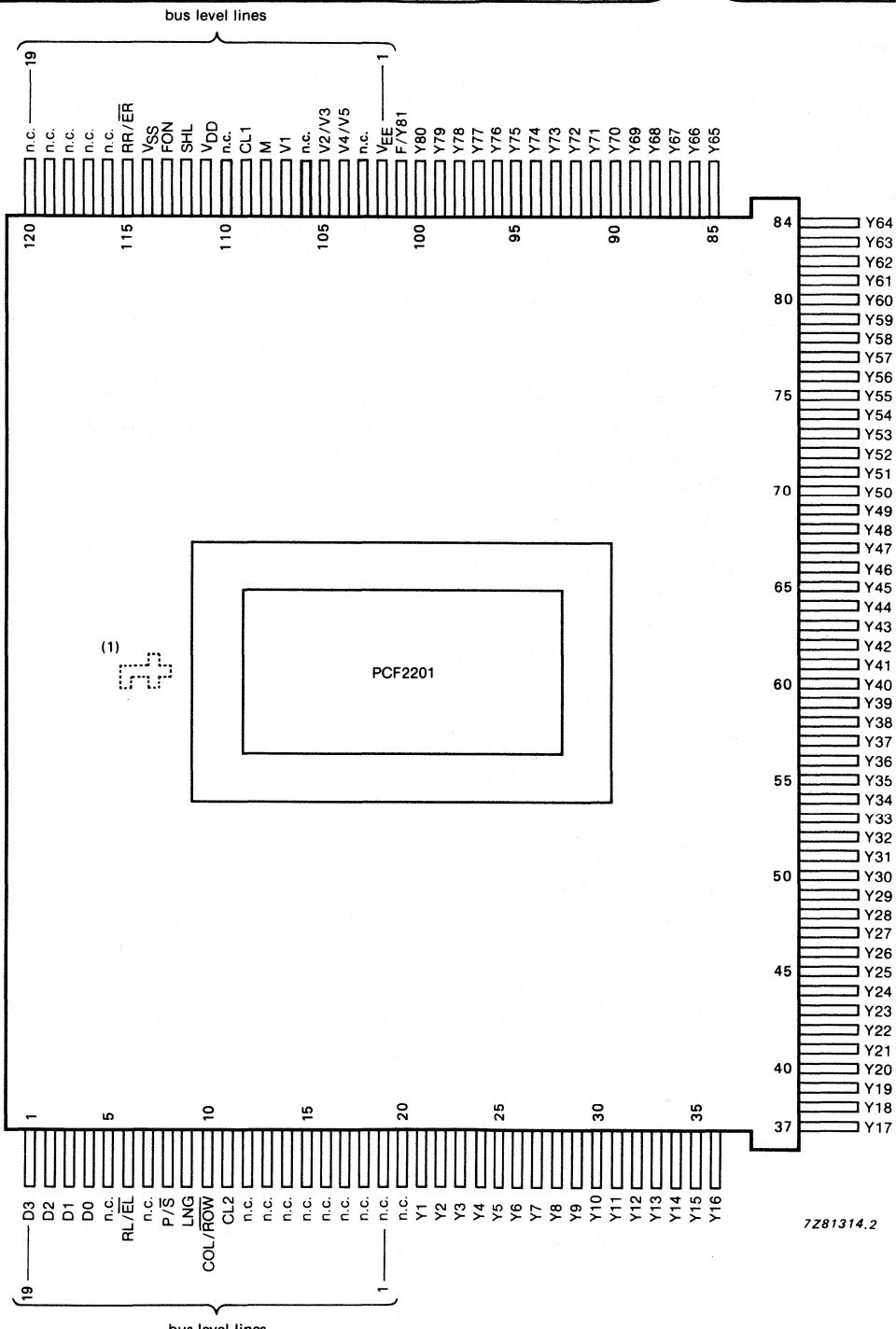


Fig. 2 Pinning diagram.

(1) mark orientation

PINNING FUNCTIONS

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>V_{DD}
V_{SS}
V_1
V_2/V_3
V_4/V_5
V_{EE}</td><td>P
P
P
P
P
P</td><td>Positive supply voltage (5 V)
Logic ground (0 V)
Most positive LCD supply voltage ($\leqslant V_{DD}$), selection level
Upper non-selection level for row (V2) or column (V3) driver
Lower non-selection level for row (V5) or column (V4) driver
Most negative LCD supply voltage (−20 V), selection level</td></tr>
<tr><td>Y1 to Y80</td><td>O</td><td>Liquid crystal driver outputs</td></tr>
<tr><td>CL1</td><td>I</td><td>Clock for 81 stage bidirectional shift register
Loads parallel data from the data presentation latch and frame control in column driver mode
Shifts data in row driver mode
Negative edge triggered</td></tr>
<tr><td>CL2</td><td>I</td><td>Data transfer clock in column driver modes
Data must be valid on the negative edge of CL2
Unused in row driver mode (may be left open)</td></tr>
<tr><td>COL/$\overline{\text{ROW}}$</td><td>I</td><td>Column/row driver mode select</td></tr>
<tr><td>P/$\overline{\text{S}}$</td><td>I</td><td>Parallel/serial mode select for column drivers
Tie to V_{SS} in row driver mode</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select</td></tr>
<tr><td>D0 to D3</td><td>I</td><td>Data inputs in column driver modes
Unused in row driver mode (may be left open)
Filling order:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>P/$\overline{\text{S}}$</th><th>SHL</th><th>D0</th><th>D1</th><th>D2</th><th>D3</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Y1, Y2, Y3,.</td><td>unused</td><td>unused</td><td>unused</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Y80, Y79,...</td><td>(may be left open)</td><td>(may be left open)</td><td>(may be left open)</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Y1, Y5, Y9,.</td><td>Y2, Y6, Y10,.</td><td>Y3, Y7, Y11,.</td><td>Y4, Y8, Y12,..</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Y80, Y76,...</td><td>Y79, Y75,....</td><td>Y78, Y74,....</td><td>Y77, Y73,.....</td></tr>
</table>
Also in the serial column driver mode, a multiple of 4 data bits must always be transferred. Add dummy bits if necessary</td></tr>
</table>

DEVELOPMENT DATA

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>RL/$\overline{EL}$
RR/$\overline{ER}$</td><td>I/O</td><td>Left/right serial input/outputs in row driver mode, left/right enable input/outputs in column driver modes
<table>
<tr><th>COL/$\overline{ROW}$</th><th>P/$\overline{S}$</th><th>SHL</th><th>RL/$\overline{EL}$</th><th>RR/$\overline{ER}$</th><th>comments</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>I</td><td>O</td><td>shift direction:
RL/$\overline{EL}$ –> RR/$\overline{ER}$ (Y1 –> F/Y81)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>O</td><td>I</td><td>shift direction:
RR/$\overline{ER}$ –> RL/$\overline{EL}$ (F/Y81 –> Y1)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 80 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 80 CL2 pulses after RR/$\overline{ER}$</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 20 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 20 CL2 pulses after RR/$\overline{ER}$</td></tr>
</table>
In the serial column mode, the device accepts one bit of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 80 bits of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data
The sequence is reset when CL1 is HIGH and CL2 is LOW

In the parallel column mode, the device accepts one nibble of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 20 nibbles of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data.
The sequence is reset when CL1 is HIGH and CL2 is LOW</td></tr>
<tr><td>LNG</td><td>I</td><td>Length control
<table>
<tr><th>COL/$\overline{ROW}$</th><th>LNG</th><th>SHL</th><th>description</th><th>valid Yi</th><th>undefined Yi</th></tr>
<tr><td>L.
L</td><td>L
L</td><td>L
H</td><td>65-bit row mode
operation</td><td>Y1...Y65
Y17...Y80, F/Y81</td><td>Y66...Y80, F/Y81
Y1...Y16</td></tr>
<tr><td>L
L</td><td>H
H</td><td>L
H</td><td>81-bit row mode
operation</td><td>Y1...Y80, F/Y81
Y1...Y80, F/Y81</td><td>–
–</td></tr>
<tr><td>H
H</td><td>L
L</td><td>L
H</td><td>64-bit column
mode operation</td><td>Y1...Y64
Y17...Y80</td><td>Y65...Y80
Y1...Y16</td></tr>
<tr><td>H
H</td><td>H
H</td><td>L
H</td><td>80-bit column
mode operation</td><td>Y1...Y80
Y1...Y80</td><td>–
–</td></tr>
</table>
In 80/81-bit operation, the device behaves as previously described
In 64/65-bit operation, the device behaves as if all resources have been reduced to 64/65 instances; i.e. 16 outputs (determined by SHL) can no longer be accessed and should be left open circuit.</td></tr>
</table>

PINNING FUNCTIONS (continued)

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>F/Y81*</td><td>O</td><td>Frame output in column driver mode
It continuously delivers the select or non-select column driver LCD voltages depending on the state of the frame control
The frame output is used to blank the flat-panel display margin outside the actual LCD matrix
Liquid crystal driver output, number 81 in row driver mode</td></tr>
<tr><td>FON</td><td>I</td><td>Frame control
Defines the contents of the shift register cell corresponding to F/Y81 in column driver mode
Tie to V_{DD} or V_{SS} in row driver mode</td></tr>
<tr><td>M</td><td>I</td><td>Signal to convert LCD drive waveform into a.c.:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>SR data</th><th>M</th><th>output level (Y_i or F/Y81)</th><th>note</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">row driver</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>V_{EE}</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">column driver</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
</table></td></tr>
<tr><td>n.c.</td><td>–</td><td>not connected</td></tr>
</table>

* Patent application pending.

FUNCTIONAL DESCRIPTION

4-level driver

One of the liquid crystal driver levels (V_1, V_2/V_3, V_4/V_5 and V_{EE}) is output onto lines Y1 to Y80 and F/Y81 depending on the state of the relevant level shifter.

Level shifter

The level shifter converts logic level driver information into LCD level selection signals. The LCD level selection signals are dependent on the contents of the 81 stage bidirectional shift register and the state of signals M and COL/$\overline{\text{ROW}}$.

81 stage bidirectional shift register

In row driver mode the bidirectional shift register is used for the row line scan. In column driver mode the bidirectional shift register is used to hold column data until the next line is assembled in the data presentation latch.

Column mode data presentation latch

The column mode data presentation latch provides temporary storage during transfer of column data required for the next row.

Data scrambler

In serial column data transfer, the data scrambler converts 1-bit data to parallel 4-bit nibbles. Data is rearranged by the data scrambler according to the orientation (left or right) of the chip, as defined by pin SHL.

Selector

The selector generates latch clocks $\phi 1$ to $\phi 20$ for the presentation latch. Selection is determined by the state of the up/down counter and the carry logic.

Up/down counter, carry logic and control

Incoming column data storage locations are determined by the up/down counter making use of enable lines (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$) and the length control select (LNG). The carry logic inhibits the data transfer clock (CL2) in inactive column drivers, thereby reducing power dissipation. When data transfer to one column driver is completed, the subsequent column driver is enabled by the carry logic. The control part co-ordinates the up/down counter and carry logic, depending upon the condition of the device (SHL, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, LNG, RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	V_{SS} −0,3 to V_{SS} + 7	V
LCD supply voltage range	V_{EE}	V_{DD} −30 to V_{DD}	V
V_1, V_2/V_3 voltage range (note 1)	V_U	$\frac{V_{DD} + V_{EE}}{2}$ −1 to V_{DD}	V
V_4/V_5 voltage range (note 1)	V_L	V_{EE} to $\frac{V_{DD} + V_{EE}}{2}$ − 1	V
Input voltage range (CL1, CL2, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, SHL, D0, D1, D2, D3, RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$, LNG, FON, M)	V_I	V_{SS} −0,3 to V_{DD} + 0,3	V
Output voltage range (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$)	V_O	V_{SS} −0,3 to V_{DD} + 0,3	V
Driver output voltage range (F/Y81, Y1 to Y80)	V_Y	V_{EE} −0,3 to V_{DD} + 0,3	V
DC input current	$\pm I_I$	max. 20	mA
DC output current	$\pm I_O$	max. 25	mA
V_{DD}, V_{SS}, V_1, V_2/V_3, V_4/V_5 or V_{EE} current	$\pm I_{SUP}$	max. 20	mA
Power dissipation per package	P_{tot}	max. 400	mW
Power dissipation per output	P_o	max. 100	mW
Storage temperature range	T_{stg}	−65 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 4,5 to 5,5 V;

V_{EE} = 0 to −20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$; f_M = 100 Hz

T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Positive supply voltage		V_{DD}	4,5	–	5,5	V
Negative LCD supply voltage		V_{EE}	V_{DD}−25	–	V_{DD}−5	V
Static supply current	$f_{CL1} = f_{CL2}$ = 0 Hz; COL/$\overline{\text{ROW}}$ = H; M = L; note 2	I_{DD1}	–	15	40	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; f_{CL1} = 25 kHz; f_{CL2} = 4 MHz; note 2	I_{DD2}	–	0,4	1	mA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; RL/$\overline{\text{EL}}$ = H (SHL = L) or RR/$\overline{\text{ER}}$ = H (SHL = H); f_{CL1} = 25 kHz; note 2	I_{DD3}	–	50	150	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = L; f_{CL1} = 100 kHz; note 2	I_{DD4}	–	75	200	μA
Logic						
Input voltage LOW HIGH		V_{IL} V_{IH}	0 0,7 V_{DD}	– –	0,3 V_{DD} V_{DD}	V
Output voltage LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	V_{OL} = 1 V	I_{OL}	1	–	–	mA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output current HIGH RL/$\overline{EL}$ and RR/$\overline{ER}$	$V_{OH} = V_{DD}-1$ V	I_{OH}	–	–	1	mA
Leakage current at CL1, CL2, COL/$\overline{ROW}$, P/$\overline{S}$, SHL, D0 to D3, RL/$\overline{EL}$, RR/$\overline{ER}$, LNG, FON and M		$\pm I_{L1}$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	7	pF
LCD outputs						
Leakage current at V_1, V_2/V_3, V_4/V_5		$\pm I_{L2}$	–	–	2	μA
Resistance ON between V_1, V_2/V_3, V_4/V_5, V_{EE} and Y1 to Y80, F/Y81	$I_O = 100$ μA; $V_{EE} = V_{DD}-25$ V note 4	R_{ON}	–	–	2	kΩ

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 4{,}5$ to $5{,}5$ V;
$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$;
$f_M = 100$ Hz; see Figs 4 and 5; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Column driver data transfer rate		f_{CL2}	–	–	4	MHz
CL2 HIGH time		t_{CL2H}	100	–	–	ns
CL2 LOW time		t_{CL2L}	100	–	–	ns
CL2 rise time		t_{CL2r}	–	–	25	ns
CL2 fall time		t_{CL2f}	–	–	25	ns
Row driver clock rate		f_{CL1}	–	–	100	kHz
CL1 HIGH time		t_{CL1H}	275	–	–	ns
CL1 LOW time		t_{CL1L}	5	–	–	μs
CL1 rise time		t_{CL1r}	–	–	50	ns
CL1 fall time		t_{CL1f}	–	–	50	ns

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Column data set-up time	COL/$\overline{\text{ROW}}$ = H	t_{SUC}	50	–	–	ns
Column data hold time	COL/$\overline{\text{ROW}}$ = H	t_{HDC}	30	–	–	ns
Row data set-up time	COL/$\overline{\text{ROW}}$ = L	t_{SUR}	200	–	–	ns
Row data hold time	COL/$\overline{\text{ROW}}$ = L	t_{HDR}	0	–	–	ns
Enable HIGH to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECH}	90	–	–	ns
Enable LOW to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECL}	85	–	–	ns
Propagation delay to enable HIGH	COL/$\overline{\text{ROW}}$ = H	t_{PEH}	–	–	185	ns
Propagation delay to enable LOW	COL/$\overline{\text{ROW}}$ = H	t_{PEL}	–	–	140	ns
CL2 to CL1 time	COL/$\overline{\text{ROW}}$ = H	t_{CL21}	50	–	–	ns
CL1 to CL2 time	COL/$\overline{\text{ROW}}$ = H	t_{CL12}	50	–	–	ns
Overlap time of CL2 = LOW and CL1 = HIGH	COL/$\overline{\text{ROW}}$ = H	t_{ov}	275	–	–	ns
Propagation delay HIGH to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PLH}	20	–	200	ns
Propagation delay LOW to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PHL}	20	–	200	ns
Propagation delay to Y1 . . . Y80, F/Y81	$V_{EE} = V_{DD} - 20$ V	t_{PY}	–	–	3	μs

Notes to characteristics

1. Maintain $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$.
2. Outputs open, inputs at V_{SS} or V_{DD}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

Fig. 3 Test loads.

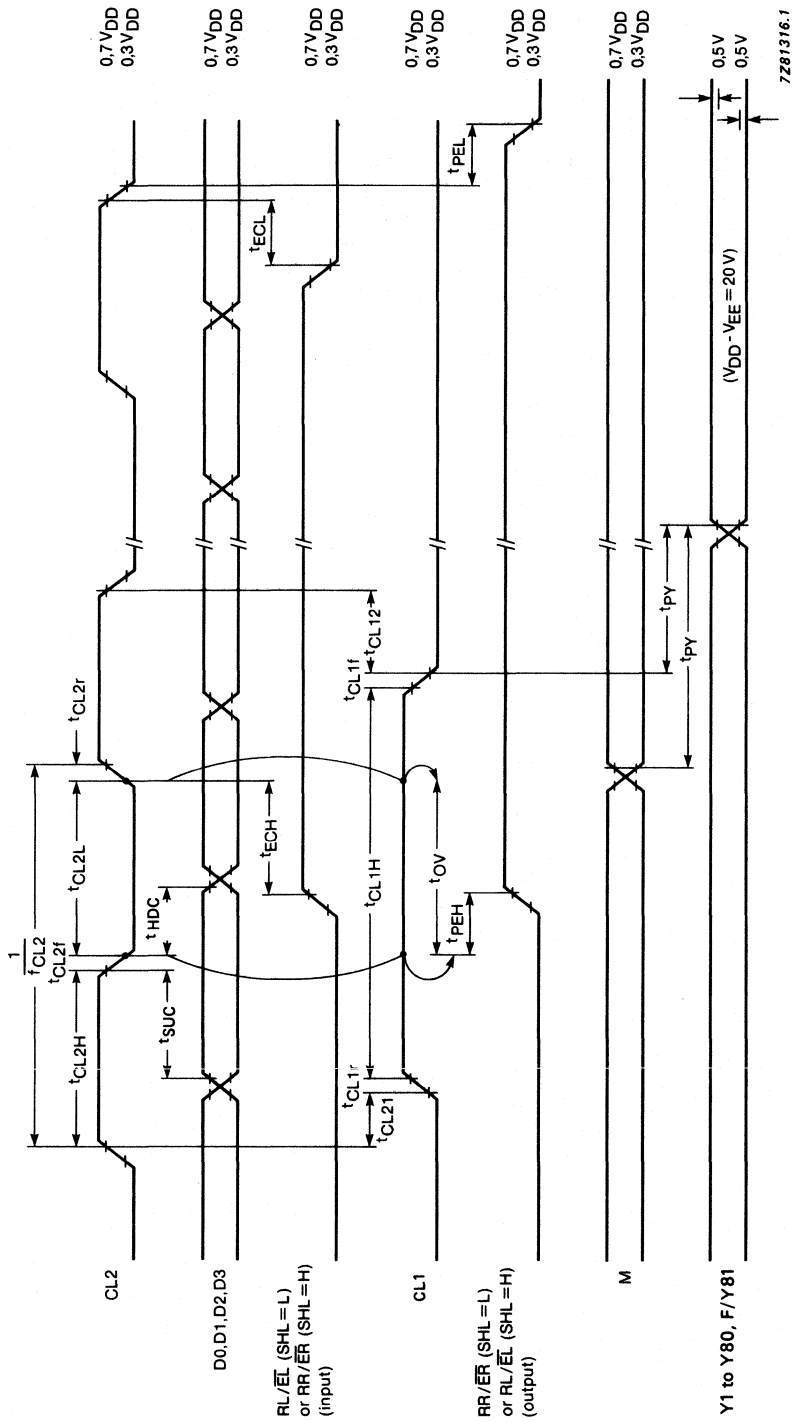


Fig. 4 Column driver timing waveforms.

DEVELOPMENT DATA

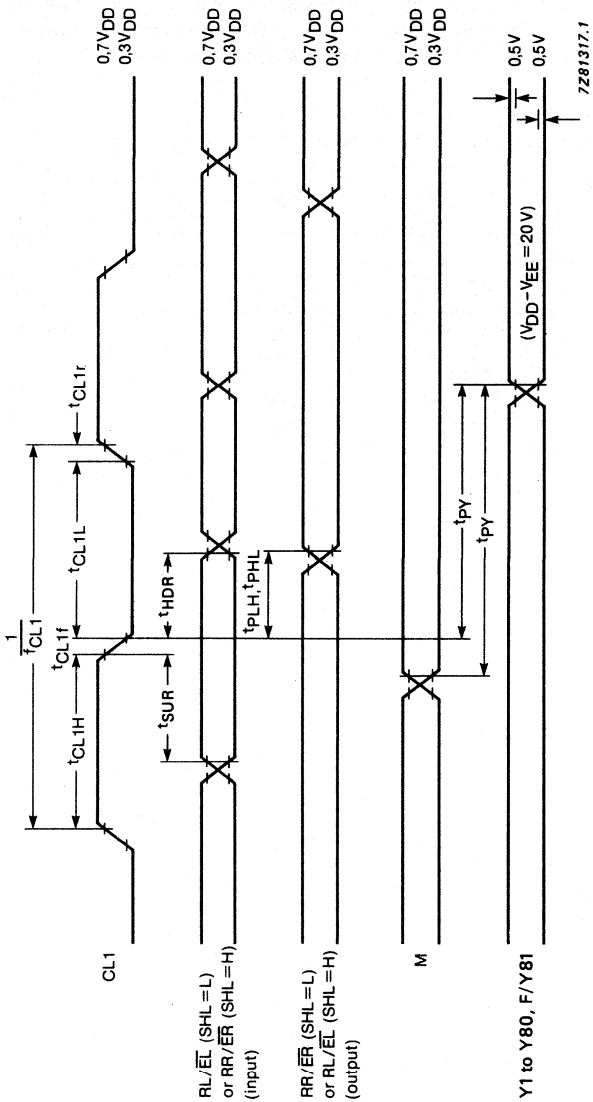


Fig. 5 Row driver timing waveforms.

APPLICATION INFORMATION

Generation of LCD bias levels

Optimum contrast for LCD flat-panels is achieved when the bias levels are selected using the formulae in Table 1. The multiplex rate is denoted by the variable n ($n \geqslant 9$). V_{th} is defined as the LCD threshold voltage, typically where the LCD exhibits approximately 10% contrast. The ratio of the 'ON' voltage to the 'OFF' voltage is discrimination (D) and is a measure of the flat-panel contrast at a given multiplex rate.

Table 1 LCD flat-panel bias levels for optimum contrast ($V_{op} = V1 - V_{EE}$)

$\frac{V_2}{V_{op}} = \frac{\sqrt{n}}{\sqrt{n}+1}$	$\frac{V_3}{V_{op}} = \frac{\sqrt{n}-1}{\sqrt{n}+1}$	$\frac{V_4}{V_{op}} = \frac{2}{\sqrt{n}+1}$	$\frac{V_5}{V_{op}} = \frac{1}{\sqrt{n}+1}$
$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$		$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n}+\frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$	
$D = \frac{V_{on(rms)}}{V_{off(rms)}} = \frac{\sqrt{n-1}}{\sqrt{n}-1}$		$\frac{V_{op}}{V_{th}} = \frac{\sqrt{n}+1}{\sqrt{2(1-1/\sqrt{n}}}$	

The intermediate bias levels are generated by a resistive divider (see Fig. 6). Capacitors (C) are used to smooth out switching transients. Considerable power consumption may result by using this arrangement when driving a large LCD flat-panel, because of the low impedance of the resistive divider.

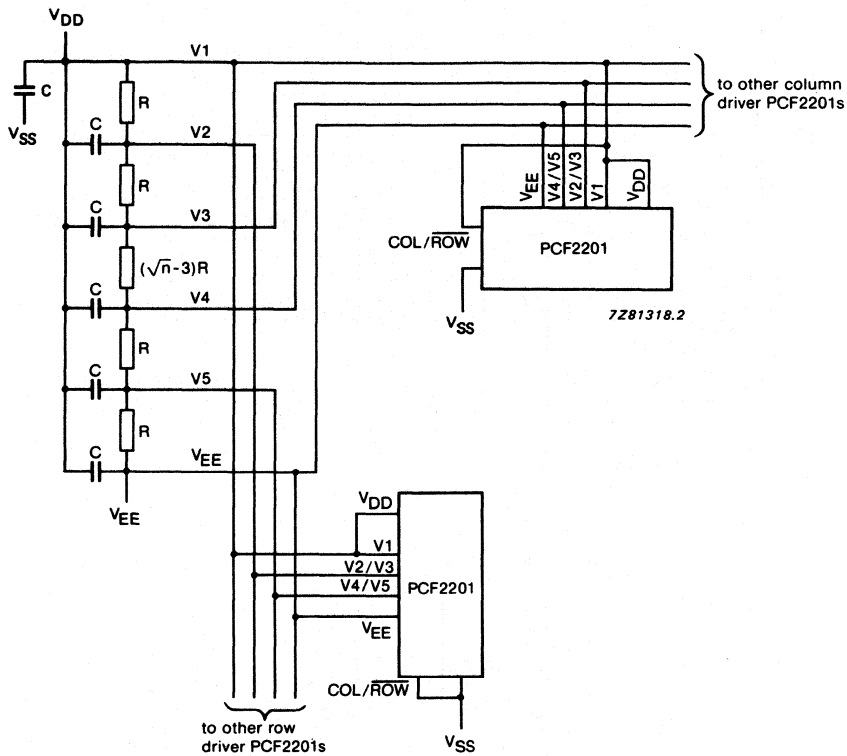


Fig. 6 Unbuffered LCD biasing level generation.

DEVELOPMENT DATA

A better solution for LCD flat-panel biasing is presented in Fig. 7. The operational amplifiers provide low impedance biasing with a low power consumption. The fairly high impedance which can be implemented at the resistive divider, helps maintain low power consumption. One diode voltage drop seperates V1 from V_{DD} to compensate for the limited common mode voltage range (V+ −1,5 V) when the operational amplifiers are powered between V_{DD} and V_{EE}.

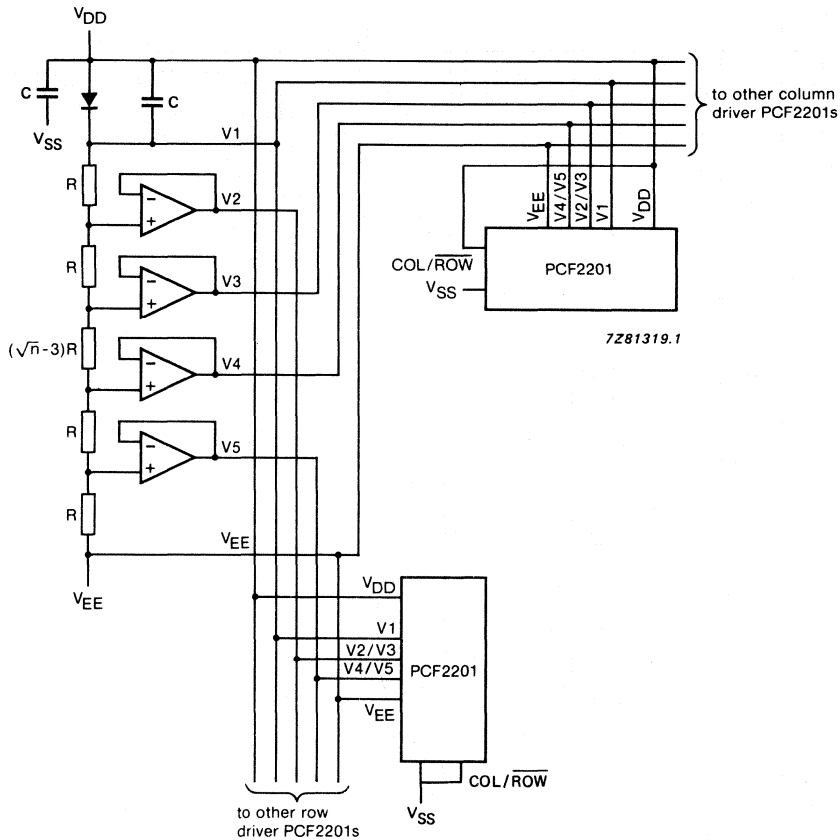


Fig. 7 Buffered LCD bias level generation.

Typical LCD flat-panel application

Alphanumeric/graphic computer terminals with LCD flat-panel screens using 200 x 640 dots are very popular. The format of 200 x 640 is compatible with the standard 25 lines by 80 characters at 8 x 8 dot character fonts. Fig. 8 gives a possible circuit using 19 PCF2201's, with upper and lower half screens used for good contrast. The use of half screens reduces the multiplex rate to 1:100 (Fig. 9 gives the timing information).

DEVELOPMENT DATA

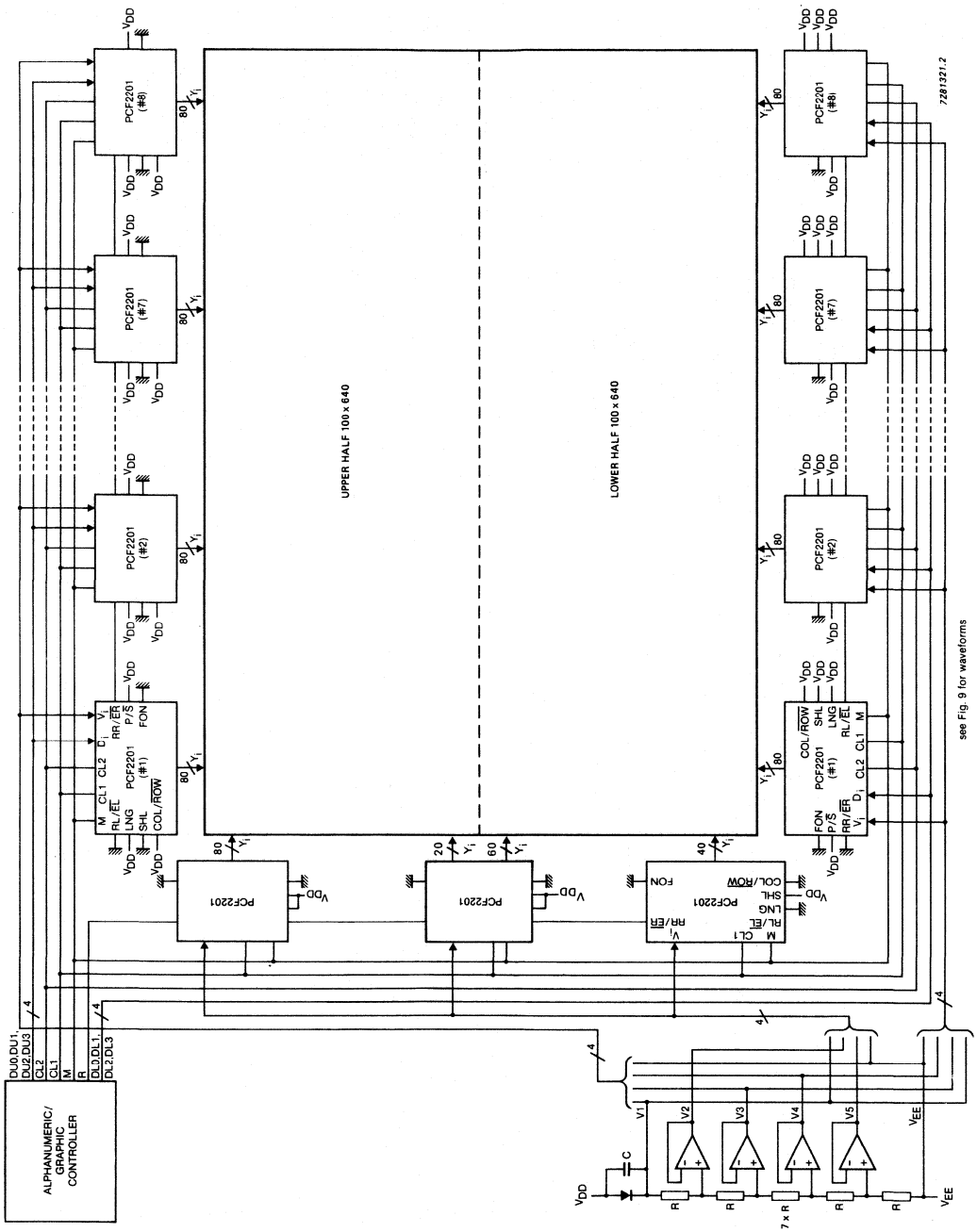


Fig. 8 LCD flat-panel with 1:100 multiplex rate in upper and lower half screens.

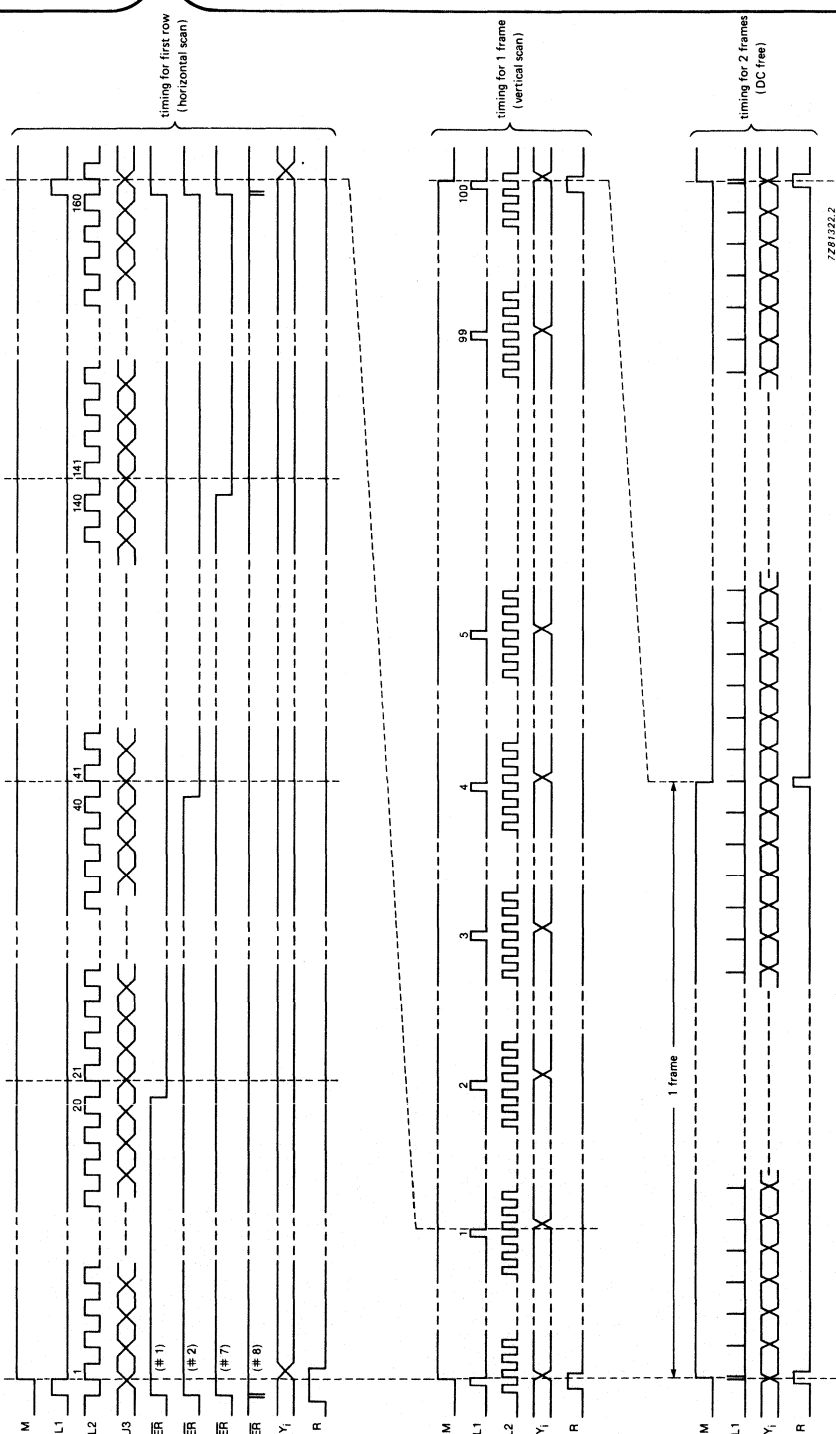
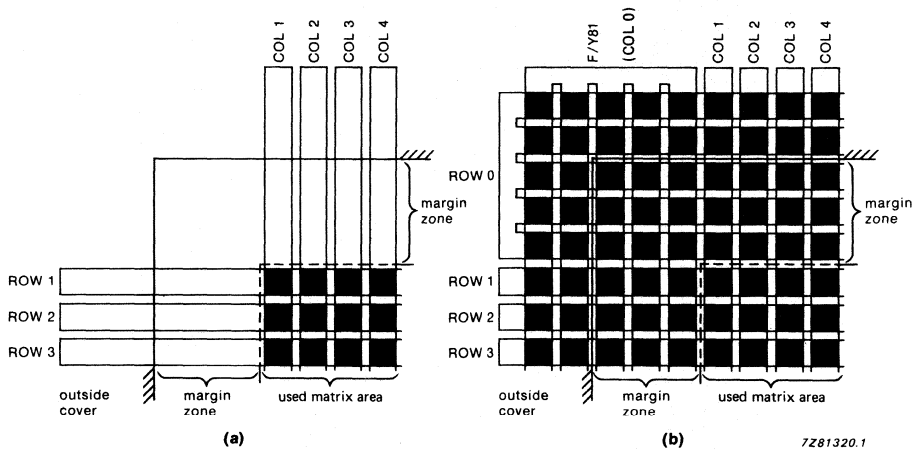


Fig. 9 Timing for the upper half screen of the LCD flat-panel (Fig. 8). For the lower half screen, replace RR/$\overline{ER}$, DU0, DU1, DU2 and DU3 with RL/$\overline{EL}$, DL0, DL1, DL2, DL3.

Margin control

The used area of the flat-panel matrix is normally smaller than the LCD glass surface. Connection lines outside of the used area of the matrix carry row or column LCD signals (see Fig. 10A). This 'null' state differs slightly in colour from the 'OFF' state pixel for twisted nematic LCD. The structural change in the margin zone is noticeable.

When a high contrast Philips LCD flat-panel of the supertwisted birefringence effect (SBE) type is employed, the situation becomes critital. The colour of the 'OFF' state appears blue and the colour of the 'ON' state appears grey or white. Therefore inverted information is sent to the display, generating dark (blue) characters on a light (grey) background. The margin zone is treated as an extension of the used matrix area (see Fig. 10B), to avoid the margin zone appearing as a dark blue frame. This is extended out to a region where the LCD glass can be covered up. The additional row requires an increase in the multiplex rate from n to n + 1, the additional column is realized by the frame output of the furthest left and right column drivers of the flat-panel. This removes the requirement for additional column drivers packages to provide margin control.



(A) without margin control

(B) with margin control

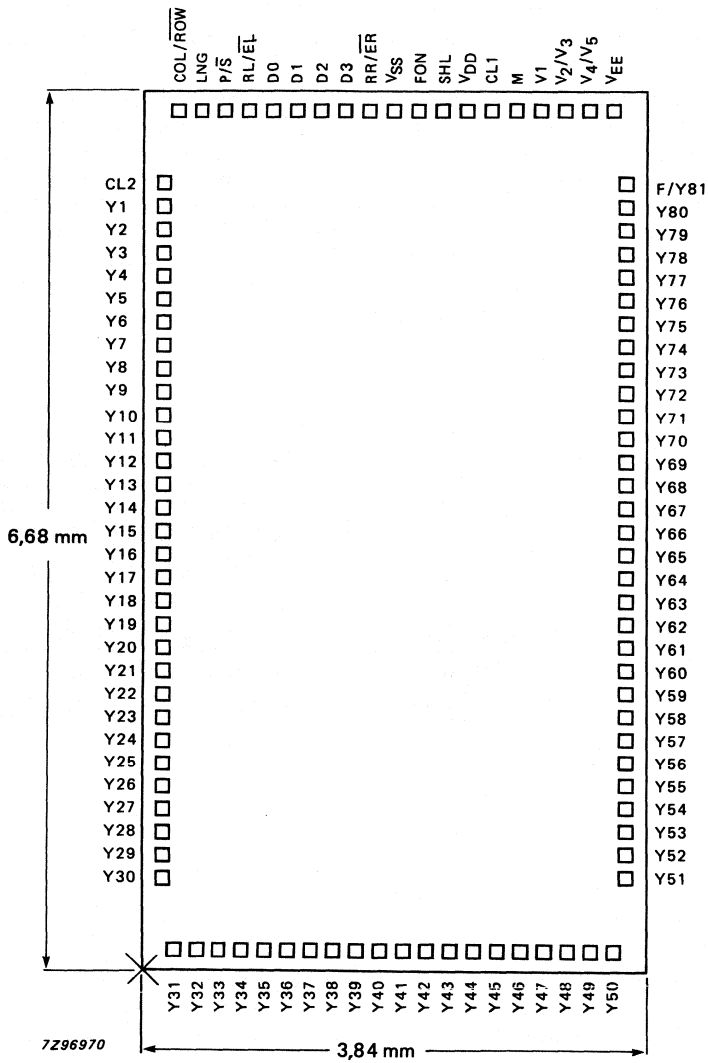
Fig. 10 Upper left corner of the LCD flat-panel.

Single plane wiring

The pinning of the PCF2201 tape-automated bonding package has been selected for ease of wiring. One side of this package contains no pins. The adjacent logic level lines are arranged so that they can be bussed in a single plane on the printed circuit board, which allows single sided substrates to be used.

For ease of wiring layout it is suggested to use the bus-level numbers (see Fig. 2) since most supply lines can be run through at the same level. On the actual package there are 120 pins, of which 19 pins are not internally connected. These extra pins are due to single plane wiring gaps and enhance stability in surface mounting.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 25,65 mm^2

Bonding pad dimensions: 104 μm x 104 μm

Fig. 11 Bonding pad locations.

Table 2 Bonding pad centre locations (dimensions in μm)

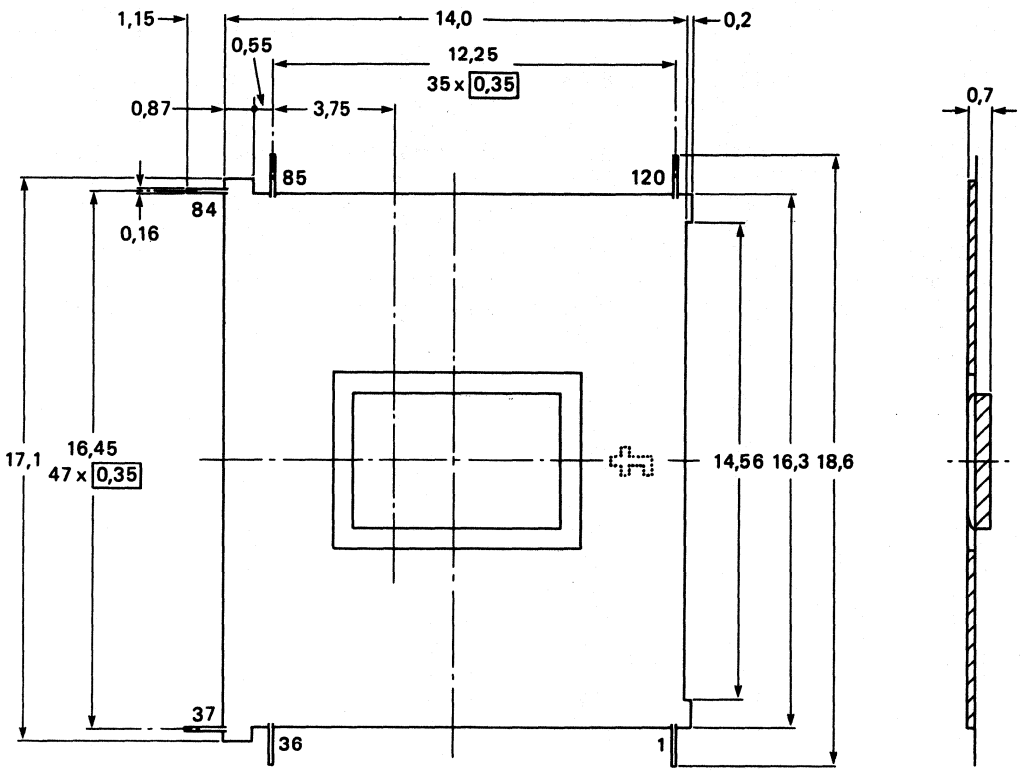
All x/y co-ordinates are referenced to the bottom left corner, see Fig. 11.

pad	X	Y	pad	X	Y
D3	1556	6526	Y43	2364	154
D2	1372	6526	Y44	2540	154
D1	1188	6526	Y45	2716	154
D0	1004	6526	Y46	2892	154
RL/$\overline{EL}$	820	6526	Y47	3068	154
P/$\overline{S}$	636	6526	Y48	3244	154
LNG	452	6526	Y49	3420	154
COL/$\overline{ROW}$	268	6526	Y50	3596	154
CL2	156	5982	Y51	3684	702
Y1	156	5806	Y52	3684	878
Y2	156	5630	Y53	3684	1054
Y3	156	5454	Y54	3684	1230
Y4	156	5278	Y55	3684	1406
Y5	156	5102	Y56	3684	1582
Y6	156	4926	Y57	3684	1758
Y7	156	4750	Y58	3684	1934
Y8	156	4574	Y59	3684	2110
Y9	156	4398	Y60	3684	2286
Y10	156	4222	Y61	3684	2462
Y11	156	4046	Y62	3684	2638
Y12	156	3870	Y63	3684	2814
Y13	156	3694	Y64	3684	2990
Y14	156	3518	Y65	3684	3166
Y15	156	3342	Y66	3684	3342
Y16	156	3166	Y67	3684	3518
Y17	156	2990	Y68	3684	3694
Y18	156	2814	Y69	3684	3870
Y19	156	2638	Y70	3684	4046
Y20	156	2462	Y71	3684	4222
Y21	156	2286	Y72	3684	4398
Y22	156	2110	Y73	3684	4574
Y23	156	1934	Y74	3684	4750
Y24	156	1758	Y75	3684	4926
Y25	156	1582	Y76	3684	5102
Y26	156	1406	Y77	3684	5278
Y27	156	1230	Y78	3684	5454
Y28	156	1054	Y79	3684	5630
Y29	156	878	Y80	3684	5806
Y30	156	702	F/Y81	3684	5982
Y31	252	154	V_{EE}	3580	6526
Y32	428	154	V_4/V_5	3396	6526
Y33	604	154	V_2/V_3	3212	6526
Y34	780	154	V1	3028	6526
Y35	956	154	M	2844	6526
Y36	1132	154	CL1	2660	6526
Y37	1308	154	V_{DD}	2476	6526
Y38	1484	154	SHL	2292	6526
Y39	1660	154	FON	2108	6526
Y40	1836	154	V_{SS}	1924	6526
Y41	2012	154	RR/$\overline{ER}$	1740	6526
Y42	2188	154			

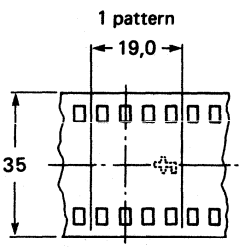
DEVELOPMENT DATA

120-LEAD TAPE-AUTOMATED BONDING PACKAGE

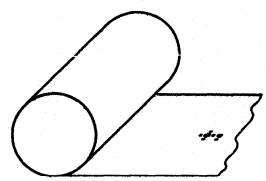
Dimensions in mm



120 lead tab module



tape



orientation on reel

7Z95862.1

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or, for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots.
The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (possible 40,960 dots)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8578U: uncased chip-in-tray.

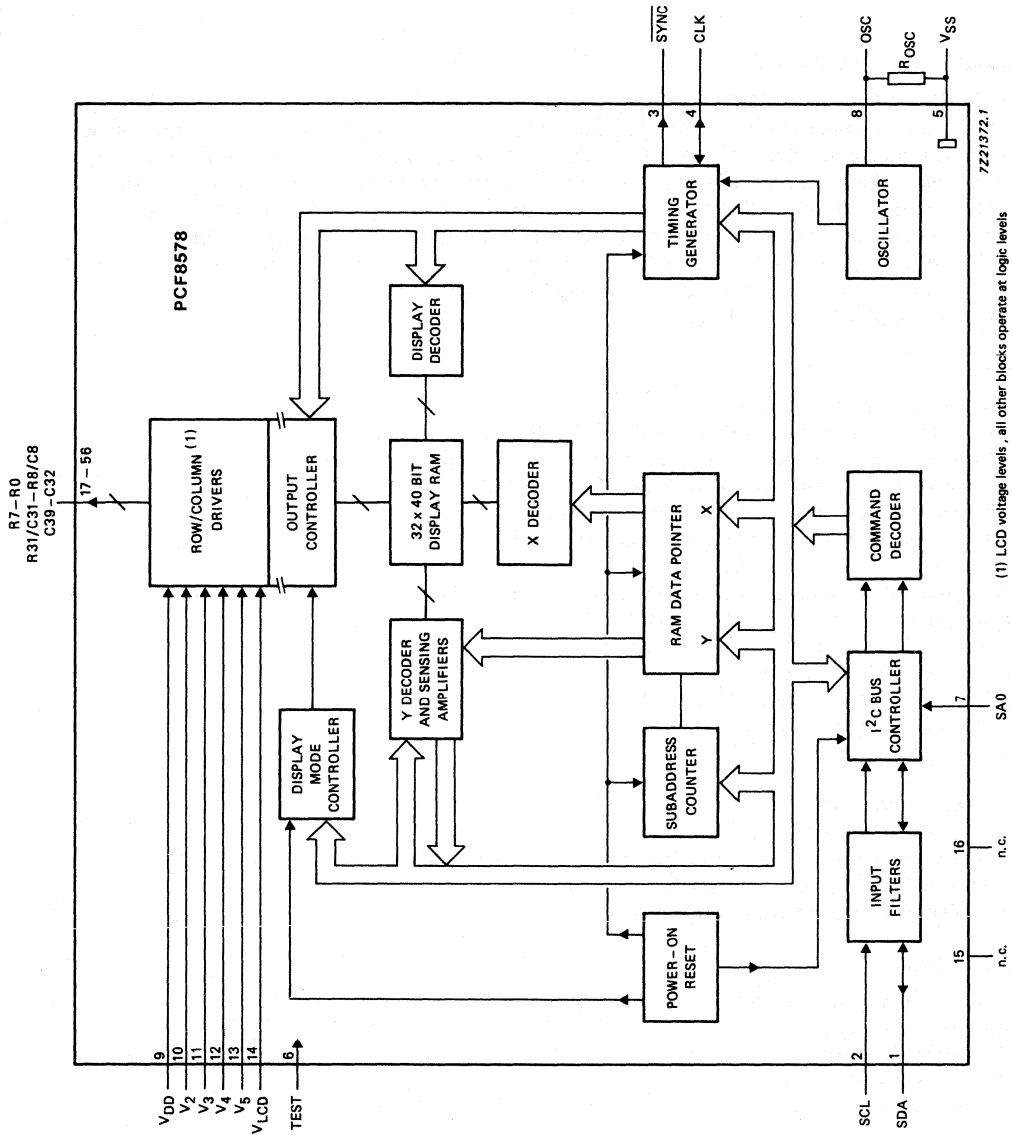


Fig. 1 Block diagram.

DEVELOPMENT DATA

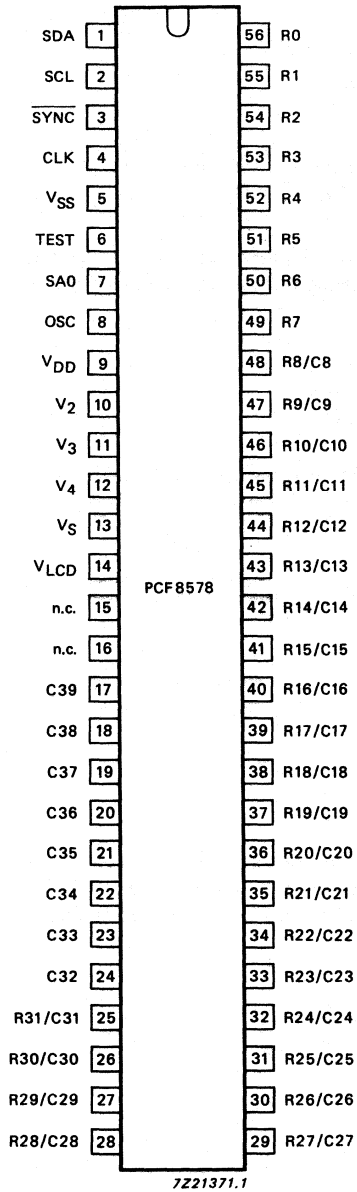


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output ⎫ I²C bus
2	SCL	Clock input ⎭
3	$\overline{SYNC}$	Cascade synchronization output
4	CLK	External clock input/output
5	V_{SS}	Ground (logic)
6	TEST	Test pin (connect to V_{SS})
7	SA0	I²C bus slave address input (bit 0)
8	OSC	Oscillator input
9	V_{DD}	Positive supply voltage
10	V_2	⎫ LCD bias voltage inputs
11	V_3	⎪
12	V_4	⎪
13	V_5	⎭
14	V_{LCD}	LCD supply voltage
15	n.c.	Not connected
16	n.c.	Not connected
17 to 24	C39 to C32	⎫ LCD column driver outputs ⎭
25 to 48	R31/C31 to R8/C8	⎫ LCD row/column driver outputs ⎭
49 to 56	R7 to R0	⎫ LCD row driver outputs ⎭

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications or for larger displays with up to 15 PCF8579s (31 when two slave addresses are used). See Table 1 for common display configurations.

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Common display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1 : 8 1 : 16 1 : 24 1 : 32	8 16 24 32	32 24 16 8	– – – –	– – – –	small digital or alphanumeric displays
with PCF8579	1 : 8 1 : 16 1 : 24 1 : 32	8 16 24 32 using 15 PCF8579s	632 624 616 608	8 x 4 16 x 2 24 32 using 16 PCF8579s	640 640 640 640	alphanumeric displays and dot matrix graphic displays

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays bias sources with high driver capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig. 3 (a stand-alone system would be identical but without PCF8579).

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

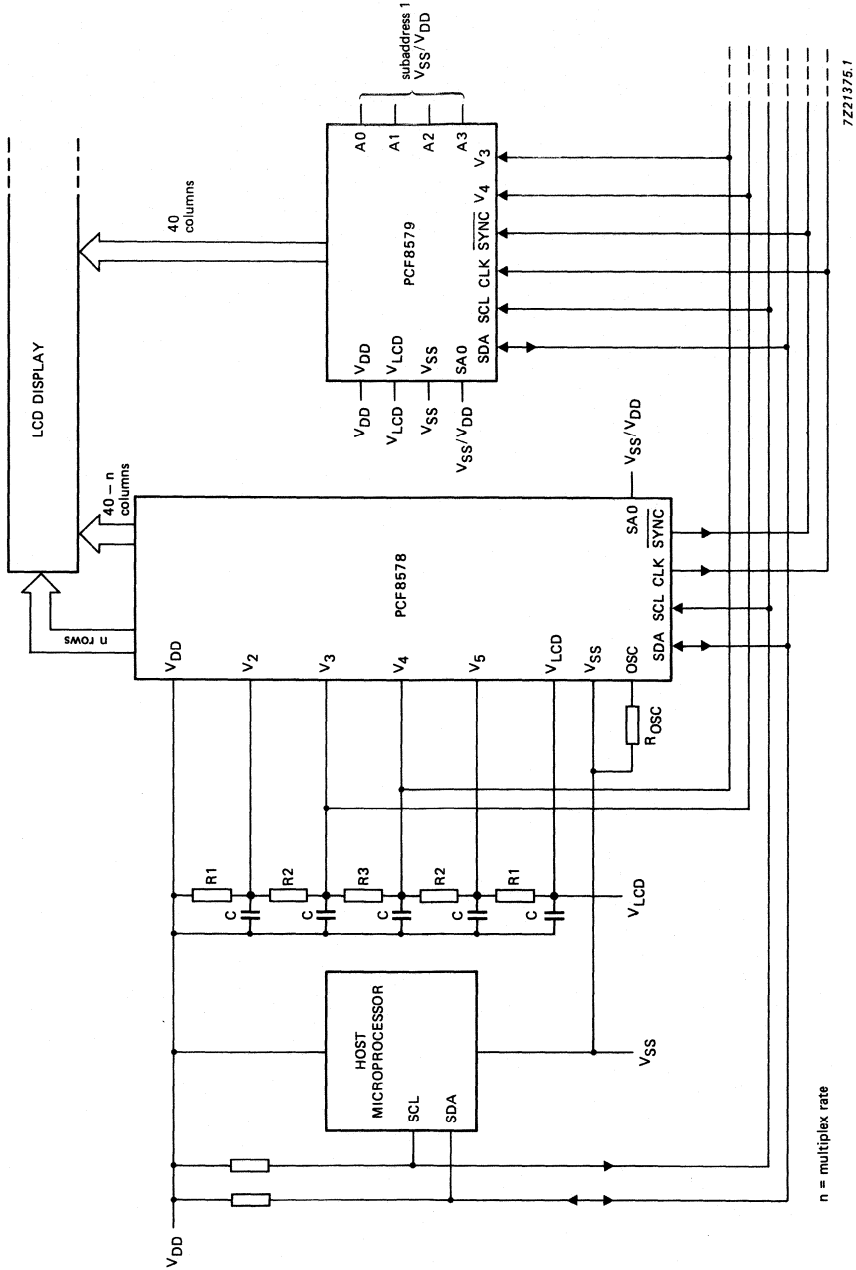


Fig. 3 Typical mixed mode configuration.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. The device is optimized for use with the PCF8578 LCD row/column driver. Up to 32 PCF8579s can be cascaded and used on the same I^2C bus (using the two slave addresses). Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8579U: uncased chip-in-tray.

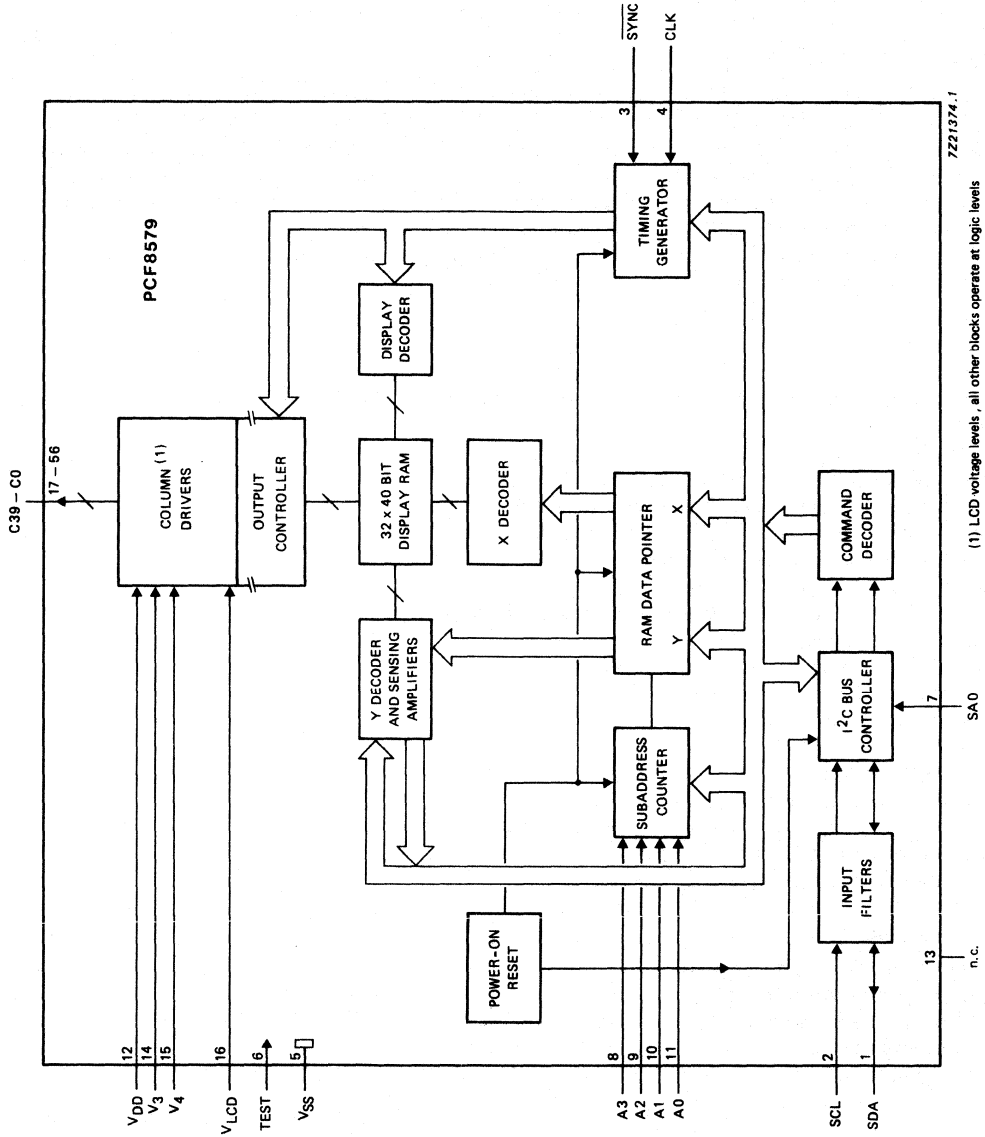


Fig. 1 Block diagram.

DEVELOPMENT DATA

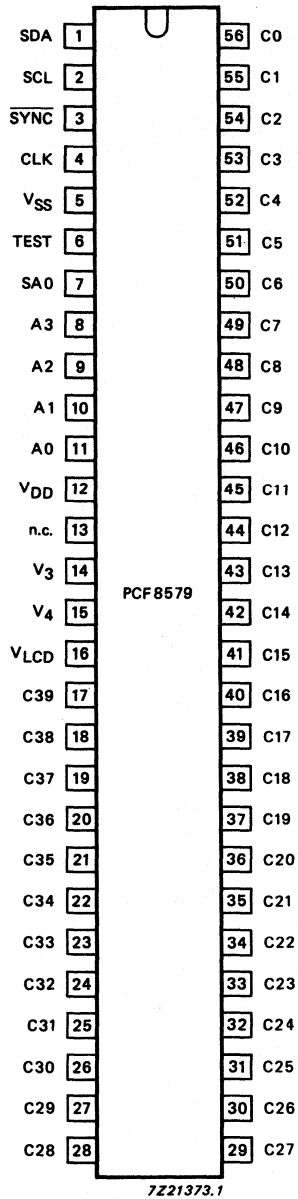


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output	I²C bus
2	SCL	Clock input	I²C bus
3	$\overline{SYNC}$	Cascade synchronization input	
4	CLK	External clock input	
5	V_{SS}	Ground (logic)	
6	TEST	Test pin (connect to V_{SS})	
7	SA0	I²C bus slave address input (bit 0)	
8	A3	I²C bus subaddress inputs	
9	A2	I²C bus subaddress inputs	
10	A1	I²C bus subaddress inputs	
11	A0	I²C bus subaddress inputs	
12	V_{DD}	Positive supply voltage	
13	n.c.	Not connected	
14	V_3	LCD bias voltage inputs	
15	V_4	LCD bias voltage inputs	
16	V_{LCD}	LCD supply voltage	
17 to 56	C39 to C0	LCD column driver outputs	

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

The PCF8578 typically operates with up to 16 PCF8579s. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s. This is achieved by setting the LSB of the I^2C bus slave address to 1 (V_{DD}) or 0 (V_{SS}) using input SA0.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. 1 : 32 multiplex rate
2. Display bank 0
3. Data pointer is set to X, Y address 0
4. Character mode
5. Subaddress counter is cleared
6. I^2C bus interface is initialized
7. Display blanked (by PCF8578)

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the threshold voltage (V_{th}). V_{th} is typically defined as the r.m.s. voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

multiplex rate	$\frac{V_1}{V_{op}}$	$\frac{V_2}{V_{op}}$	$\frac{V_3}{V_{op}}$	$\frac{V_4}{V_{op}}$	$\frac{V_{off}}{V_{op}}$	$\frac{V_{on}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	$\frac{V_{op}}{V_{th}}$
1 : 8	0,739	0,522	0,478	0,261	0,297	0,430	1,477	3,37
1 : 16	0,800	0,600	0,400	0,200	0,245	0,316	1,291	4,08
1 : 24	0,830	0,661	0,339	0,170	0,214	0,263	1,230	4,68
1 : 32	0,850	0,700	0,300	0,150	0,193	0,230	1,196	5,19

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

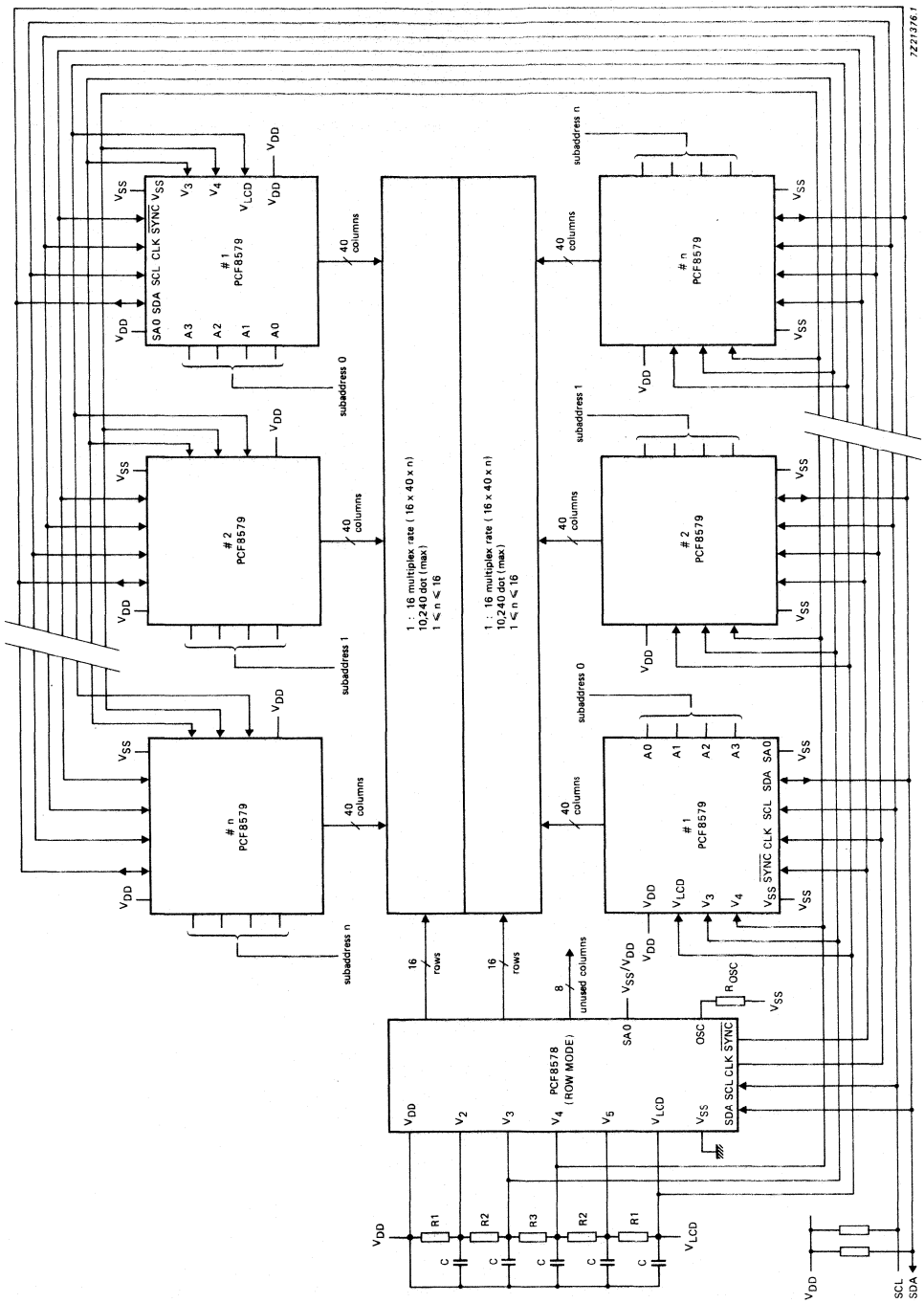


Fig. 3 Example of split screen application with 1 : 16 multiplex rate for improved contrast.

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_C) when in pointer or thermometer mode.

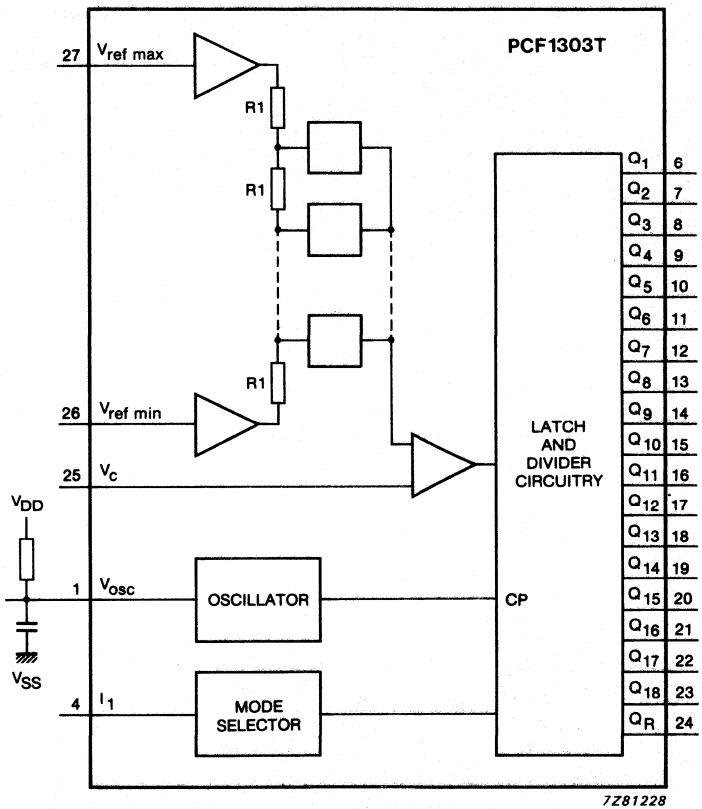
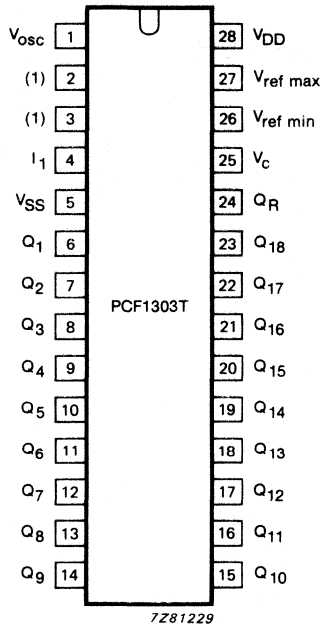


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO-28; SOT-136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\ min}$ $V_{ref\ max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

FUNCTIONAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to the control voltage when in pointer or thermometer mode.

The first segment will energize when the control voltage is less than the trigger voltage ($V_{T(bar)2}$ see equation [3]).

The circuit has analogue and digital sections.

The analogue section consists of a comparator with the inverting input coupled to the input control voltage. The non-inverting input of the comparator is connected via 17 analogue switches to the nodes of an 18-element resistor divider. The extremities of the resistor divider are coupled via high-input impedance amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The control input functions with Schmitt trigger action.

The digital section has one reference output (Q_R) to drive the back-plane and 18 outputs (Q_1 to Q_{18}) to drive the segments.

The segment outputs incorporate two latches and some gates.

The circuit is driven by an on-chip oscillator with external resistors and capacitors. The outputs are driven at typical 100 Hz.

LINEARITY

$$V_{step} = V_{step'} \pm \Delta V_{step} \qquad [1]$$

$V_{step'}$ is the voltage drop (internal) across the resistor-ladder network.
ΔV_{step} is the differential on V_{step}.

$$V_{step'} = \frac{(V_{ref\,max} \pm \Delta V_{2'}) - (V_{ref\,min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 and $\Delta V_{2'}$ are the maximum offset voltage spread of the on-chip voltage followers.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$;

$$V_{T(bar)n} = (V_{ref\,min} \pm \Delta V_{2}^{*}) + \{(n-1)V_{step'} \pm \Delta V_R\} \pm \Delta V_1 \pm V_H \qquad [3]$$

n = number of segments; $2 \leqslant n \leqslant 18$.

ΔV_R is the voltage deviation at step n of the resistor-ladder network (for n = 2 or 18, $\Delta V_R = \Delta V_{step}$).

ΔV_1 is the offset voltage for the on-chip comparator.

V_H is the hysteresis voltage: $30\%\ V_{step} \geqslant V_H \geqslant 10\%\ V_{step}$.

* For ΔV_2 the same sign (+ or −) should be used as in equation [2].

RATINGS

Limiting values as in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 15 V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5 V
D.C. current into any input or output	$\pm I_I$	max. 10 mA
Storage temperature range	T_{stg}	−25 to + 125 °C
Operating ambient temperature range	T_{amb}	−40 to + 85 °C

D.C. CHARACTERISTICS

V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C)							unit	notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Quiescent device current	10,0	I_{DD}		1200			1200		1200	µA	1
Operating supply current	8,2	I_{DD}		2,0			2,0		2,0	mA	2
Input leakage current	6,0 8,2 10,0	$\pm I_I$ $\pm I_I$ $\pm I_I$		300 300 300			300 300 300		1000 1000 1000	nA nA nA	3
HIGH level input voltage select input I_1	6,0 8,2 10,0	V_{IH} V_{IH} V_{IH}	4,2 5,8 7,0		4,2 5,8 7,0			4,2 5,8 7,0		V V V	
LOW level input voltage select input I_1	6,0 8,2 10,0	V_{IL} V_{IL} V_{IL}		1,8 2,4 3,0	2,4		1,8 2,4 3,0		1,8 3,0	V V V	
HIGH level output voltage	6,0 8,2 10,0	V_{OH} V_{OH} V_{OH}	5,95 8,15 9,95		5,95 8,15 9,95			5,95 8,15 9,95		V V V	4
LOW level output voltage	6,0 8,2 10,0	V_{OL} V_{OL} V_{OL}		0,05 0,05 0,05			0,05 0,05 0,05		0,05 0,05 0,05	V V V	4
Output current HIGH	6,0 8,2 10,0	$-I_{OH}$ $-I_{OH}$ $-I_{OH}$	0,6 0,85 1,0		0,5 0,7 0,85			0,35 0,45 0,6		mA mA mA	5
Output current LOW	6,0 8,2 10,0	I_{OL} I_{OL} I_{OL}	0,65 1,0 1,3		0,5 0,8 1,0			0,4 0,6 0,8		mA mA mA	6

For notes see page 6.

parameter	V_{DD} V	symbol	T_{amb} (°C)							unit	notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Input voltage control input V_c	6,0 8,2 10,0	V_{IC} V_{IC} V_{IC}	0,0 0,0 0,0	6,0 8,2 10,0	0,0 0,0 0,0		6,0 8,2 10,0	0,0 0,0 0,0	6,0 8,2 10,0	V V V	
Input voltage $V_{ref\,max}$ input	6,0 8,2 10,0	$V_{IR\,max}$ $V_{IR\,max}$ $V_{IR\,max}$	3,6 3,6 3,6	5,5 7,7 9,5	3,6 3,6 3,6		5,5 7,7 9,5	3,6 3,6 3,6	5,5 7,7 9,5	V V V	
Input voltage $V_{ref\,min}$ input	6,0 8,2 10,0	$V_{IR\,min}$ $V_{IR\,min}$ $V_{IR\,min}$	0,5 0,5 0,5	1,0 4,5 6,0	0,5 0,5 0,5		1,0 4,5 6,0	0,5 0,5 0,5	1,0 4,5 6,0	V V V	
$V_{ref\,max} - V_{ref\,min}$	6,0 8,2 10,0	ΔV_I ΔV_I ΔV_I	3,0 3,0 3,0		3,0 3,0 3,0			3,0 3,0 3,0		V V V	
DC component bar output to back-plane output	8,2	$\pm V_{BP}$		25		10	25		25	mV	7
Back-plane frequency	8,2	f_{BP}	90	110		100		90	110	Hz	8
Input offset voltage	8,2	$\pm V_{IO}$		120			120		120	mV	9
Step voltage variation	8,2	$\pm \Delta V_{step}$		50			50		50	mV	10
Input voltage slew rate V_c input	6,0 8,2 10,0	SR SR SR		50 50 50			50 50 50		50 50 50	V/s V/s V/s	11

For notes see next page.

Notes to D.C. characteristics

1. $V_{ref\,min}$ = 0,5 V, $V_{ref\,max}$ = 9,5 V, $V_c = V_{osc}$ = 0 V, I_1 at V_{SS} or V_{DD}.
2. See Fig. 2.
3. Pin under test at V_{SS} or V_{DD}. All other inputs simultaneously at V_{SS} or V_{DD}.
4. I_O = 0, all inputs at V_{SS} or V_{DD}.
5. $V_{OH} = V_{DD} - 0{,}5$ V, all inputs at V_{SS} or V_{DD}.
6. V_{OL} = 0,4 V, all inputs at V_{SS} or V_{DD}.
7. f_{BP} = 100 Hz, load segment outputs to back-plane output.
   $C_1 - C_{18} \leqslant 0{,}01\ \mu F$, $C_{BP} = C_1 + C_2 + \ldots C_{18} \leqslant 0{,}05\ \mu F$, $R_1 - R_{18} \geqslant 2\ M\Omega$.
8. R_{osc} = 0,1 MΩ, C_{osc} = 390 pF.
9. Number of segments 2 or 18.
   For n = 2:

$$V_{IO} = V_c - V_{ref\,min} - \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$

   For n = 18:

$$V_{IO} = V_c - V_{ref\,max} + \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$

10. See equation [1].
11. Condition applies with clock oscillator such that f_{BP} = 100 Hz.

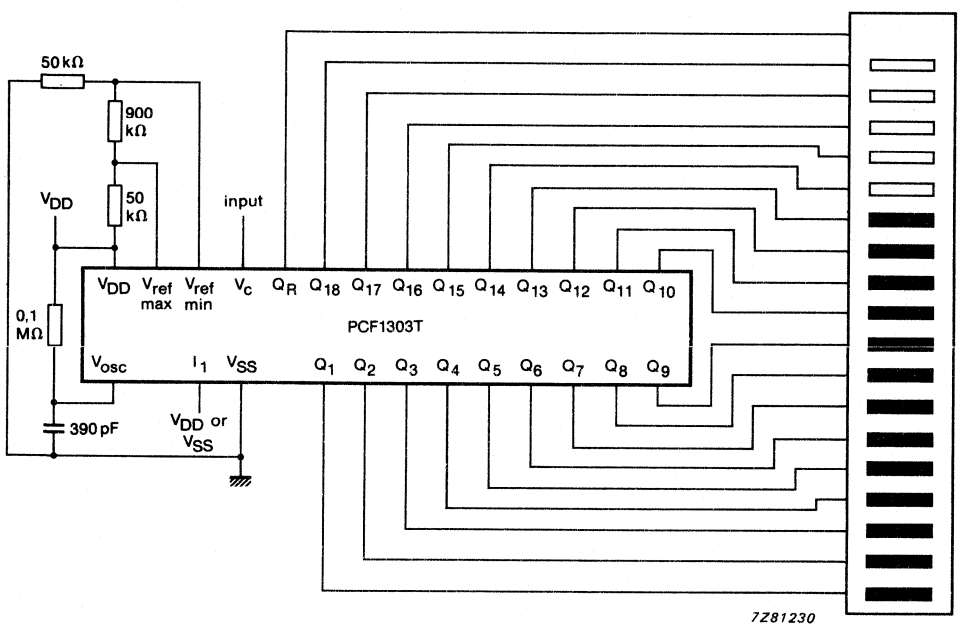


Fig. 3 Typical application.

18-ELEMENT BAR GRAPH LCD DRIVER

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_C) in a pointer or thermometer mode.

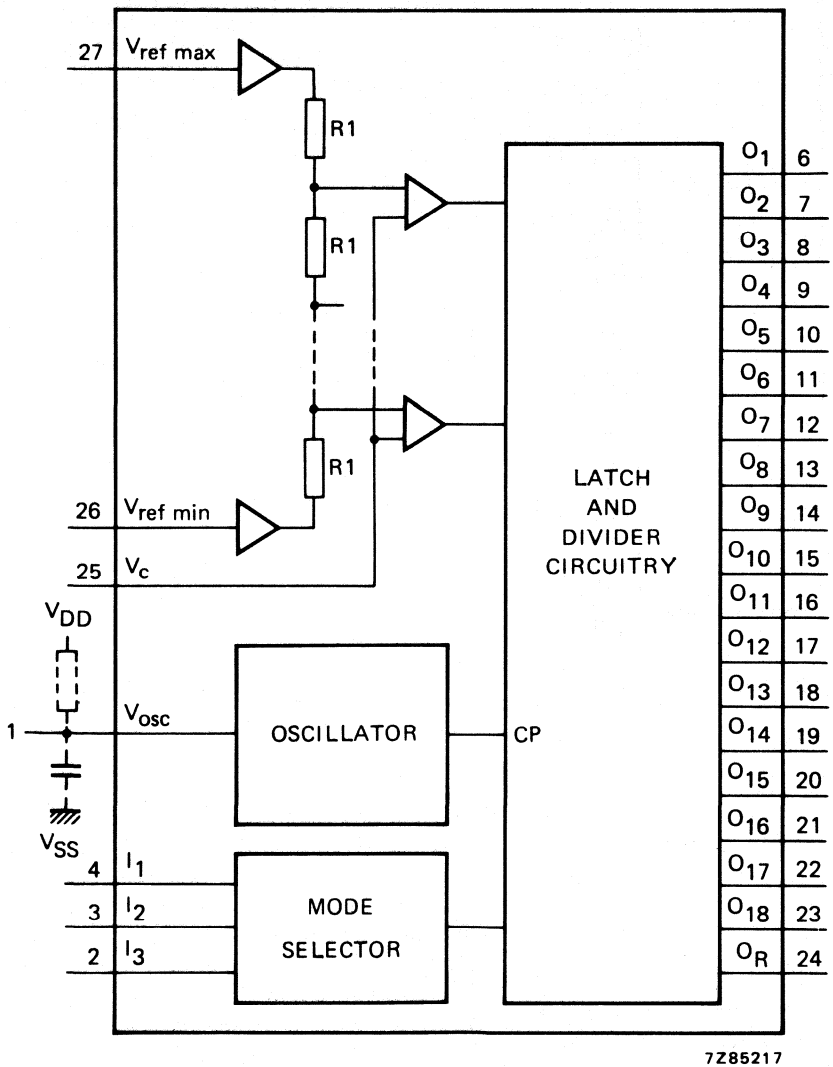


Fig. 1 Functional diagram.

FAMILY DATA see Family Specifications

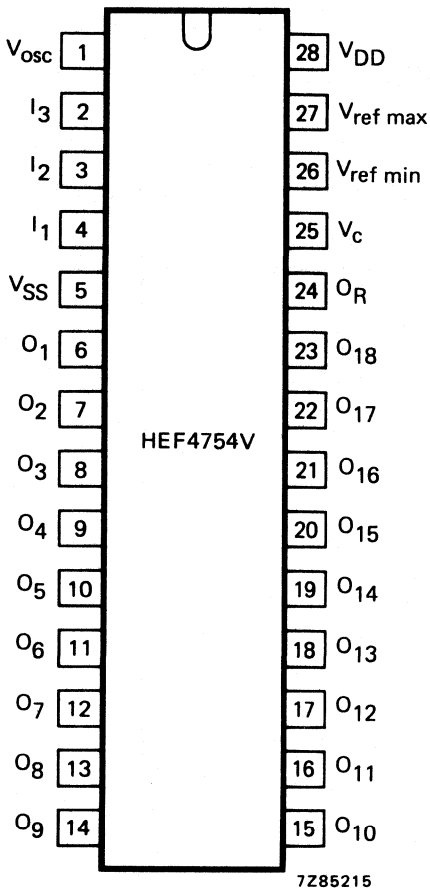


Fig. 2 Pinning diagram.

PINNING

V_{osc}	oscillator terminal
V_c	control voltage input
$V_{ref\ min}$, $V_{ref\ max}$	reference voltage inputs
I_1	thermometer/pointer (choice select input)
I_2	peak value; reset/9 or 18 bars (choice select input)
I_3	reset; repetitively reset (choice select input)
O_1 to O_{18}	bar outputs
O_R	back plate output

HEF4754VP : 28-lead DIL; plastic (SOT-117).
HEF4754VD: 28-lead DIL; ceramic (cerdip) SOT-135A).
HEF4754VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FUNCTION TABLE

I_1	I_2	I_3	mode
L	L	X	pointer; 18 bars
L	H	X	pointer; 9 bars
H	L	X	thermometer; no peak value
H	H	L	thermometer; peak value, repetitively reset
H	H	H	thermometer; peak value, manually reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

GENERAL DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode. The first bar lights up when V_c is smaller than $V_{T(bar)2}$ (see equation [3] below).

In the pointer mode, the circuit can drive 9 or 18 bars; in the thermometer mode, the circuit also drives the peak value indication. This can be reset or repetitively reset, after 1,5 to 2 seconds.

The circuit has analogue and digital parts. The analogue part consists of 17 comparators, with their non-inverting inputs connected together and coupled to the control input V_c. The inverting inputs of the comparators are connected in succession to the nodes of an 18-part resistor divider. The distance between the switching levels of the comparators is defined by the voltage difference across this divider. The extremities of the resistor divider are coupled via high-input amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The digital part has one reference output (O_R) to drive the back plate, and 18 outputs (O_1 to O_{18}) to drive each bar. Three latches and some gates are incorporated for each bar output. An on-chip oscillator (1024 Hz) with external R and C drives the circuit. The outputs are driven at 64 Hz. The select inputs I_1 to I_3 are provided with an on-chip pull-up element, and they may therefore be left floating (equals HIGH state).

LINEARITY

V_{DD} = 10 V; $V_{ref\ max}$ = 9,5 V; $V_{ref\ min}$ = 0,5 V; T_{amb} = 25 °C

ΔV_1 = 250 mV (this is the tolerance of the step voltage).

$$V_{step} = V_{step}' + \Delta V_1 \qquad [1]$$

V_{step}' is the (internal) voltage drop across the resistor-ladder network.

$$V_{step}' = \frac{(V_{ref\ max} \pm \Delta V_2) - (V_{ref\ min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 is the maximum offset voltage spread of the on-chip voltage follower.

ΔV_2 = 250 mV.

The linearity is guaranteed for $V_{DD} > 10$ V.
The monotony between V_{DD} = 5 V and 10 V is guaranteed. During ramping-up of the input voltage a maximum of two bars might be activated simultaneously.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$;

$$V_{T(bar)n} = (V_{ref\ min} \pm \Delta V_2^*) + \{(n-1)\ V_{step}' \pm \Delta V_1\}, \text{ in which} \qquad [3]$$

n = number of bars; $2 \leqslant n \leqslant 18$.

For n = 1 (first bar) see text above.

* For ΔV_2 the same sign (+ or −) should be used as in equation [2].

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 18	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	$\pm I_I$	max. 10	mA
Storage temperature	T_{stg}	−25 to + 125	°C
Operating ambient temperature	T_{amb}	−20 to + 85	°C

NOTES (to D.C. CHARACTERISTICS)

1. $V_{ref\ min}$ = 0,5 V; $V_{ref\ max}$ = 9,5 V; V_{osc} = V_c = 0 V; I_1, I_2 and I_3 at V_{DD}.
2. Pin under test at V_{SS} or V_{DD}, all other inputs simultaneously at V_{SS} or V_{DD}.
3. I_O = 0; all inputs at V_{SS} or V_{DD}.
4. At V_{DD} = 5 V: V_{OH} = 4,5 V.
   At V_{DD} = 10 V: V_{OH} = 9,5 V.
   At V_{DD} = 15 V: V_{OH} = 13,5 V.
5. At V_{DD} = 5 V: V_{OL} = 0,4 V; inputs at V_{SS} or V_{DD}.
   At V_{DD} = 10 V: V_{OL} = 0,5 V; inputs at V_{SS} or V_{DD}.
   At V_{DD} = 15 V: V_{OL} = 1,5 V; inputs at V_{SS} or V_{DD}.
6. $V_{ref\ min} + 4\ V < V_{ref\ max}$.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C)								notes
			−40		+ 25			+ 85			
			min.	max.	min.	typ.	max.	min.	max.		
Quiescent device current	5	I_{DD}	–	–	–	–	–	–	–	μA	
	10		–	–	–	–	1000	–	–	μA	1
	15		–	–	–	–	1600	–	–	μA	
Input leakage current (except select inputs)	5	$\pm I_{IN}$	–	–	–	–	100	–	–	nA	
	10		–	–	–	–	100	–	–	nA	2
	15		–	–	–	–	100	–	–	nA	
Input voltage HIGH select inputs	5	V_{IH}	3,5	–	3,5	–	–	3,5	–	V	
	10		7,0	–	7,0	–	–	7,0	–	V	
	15		11,0	–	11,0	–	–	11,0	–	V	
Input voltage LOW select inputs	5	V_{IL}	–	1,5	–	–	1,5	–	1,5	V	
	10		–	3,0	–	–	3,0	–	3,0	V	
	15		–	4,0	–	–	4,0	–	4,0	V	
Output voltage HIGH	5	V_{OH}	4,99	–	4,99	–	–	4,95	–	V	
	10		9,99	–	9,99	–	–	9,95	–	V	3
	15		–	–	14,99	–	–	–	–	V	
Output voltage LOW	5	V_{OL}	–	0,01	–	–	0,01	–	0,05	V	
	10		–	0,01	–	–	0,01	–	0,05	V	3
	15		–	0,01	–	–	0,01	–	0,05	V	
Output current HIGH	5	$-I_{OH}$	0,36	–	0,3	–	–	0,24	–	mA	
	10		0,80	–	0,7	–	–	0,56	–	mA	4
	15		3,0	–	2,8	–	–	2,60	–	mA	
Output current LOW	5	I_{OL}	0,34	–	0,3	–	–	0,24	–	mA	
	10		1,00	–	0,9	–	–	0,72	–	mA	5
	15		4,40	–	4,0	–	–	3,20	–	mA	
Input voltage control input V_C	5	V_{IC}	–	–	0	–	5	–	–	V	
	10		–	–	0	–	10	–	–	V	6
	15		–	–	0	–	15	–	–	V	
Max. input voltage $V_{ref\,max}$ input	5	V_{IRmax}	–	–	4,5	–	4,5	–	–	V	
	10		–	–	4,5	–	9,5	–	–	V	6
	15		–	–	4,5	–	14,5	–	–	V	
Min. input voltage $V_{ref\,min}$ input	5	V_{IRmin}	–	–	0,5	–	0,5	–	–	V	
	10		–	–	0,5	–	5,5	–	–	V	6
	15		–	–	0,5	–	10,5	–	–	V	
Operating supply current	10	I_{DD}	–	–	–	750	–	–	–	μA	Fig. 3

For notes see opposite page.

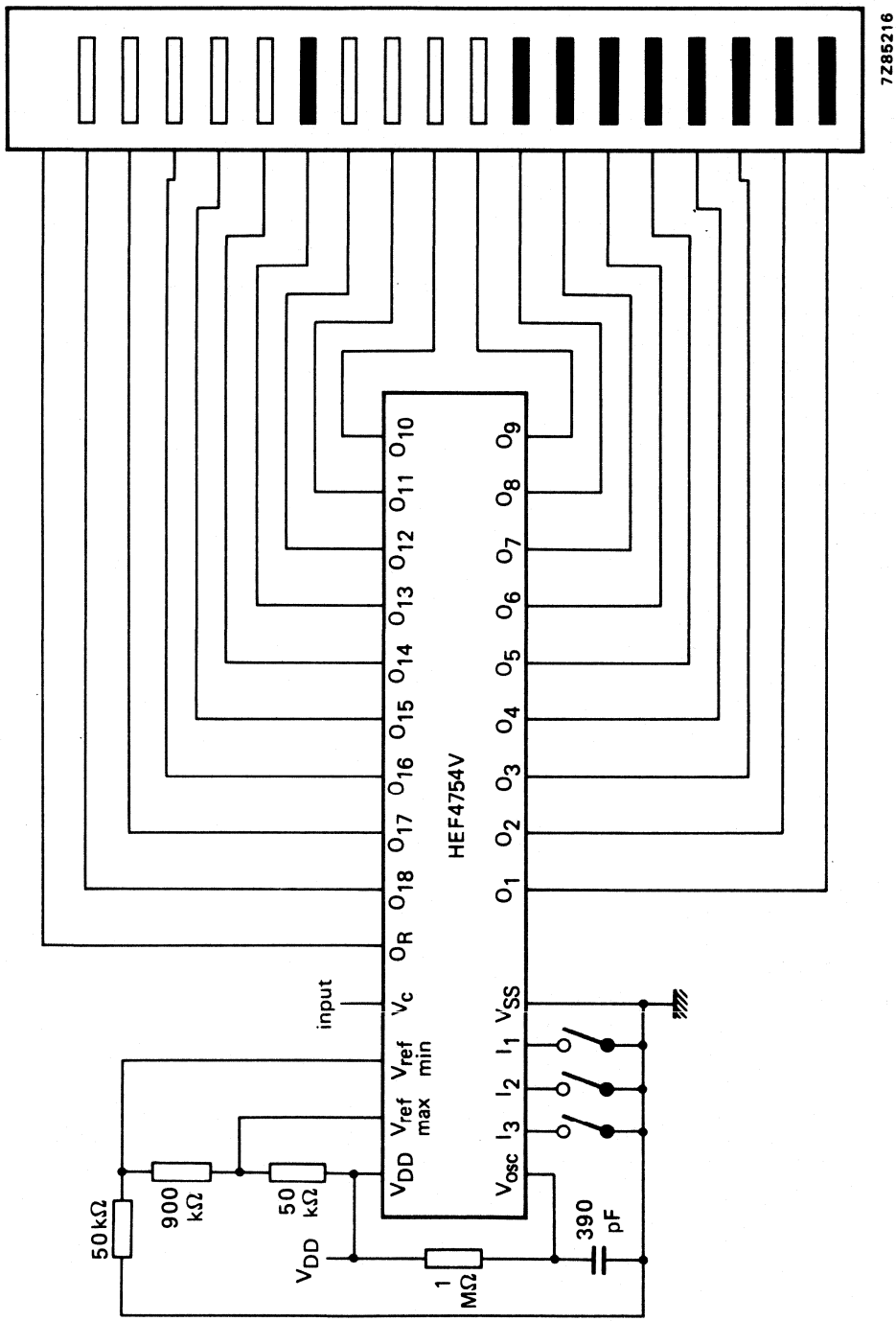


Fig. 3 Typical operating set-up.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LCDs

FEATURES

- **Latch storage of BCD inputs**
- **Blanking inputs**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have four address inputs (D_0 to D_3), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q_a to Q_g).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n LD to Q_n BI to Q_n	C_L = 15 pF V_{CC} = 5 V	29 32 20	33 31 28	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4543P: 16-lead DIL; plastic (SOT-38Z).
PC74HC/HCT4543T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	latch disable input (active HIGH)
5, 3, 2, 4	D_0 to D_3	address (data) inputs
6	PH	phase input (active HIGH)
7	BI	blanking input (active HIGH)
8	GND	ground (0 V)
9, 10, 11, 12 13, 15, 14	Q_a to Q_g	segment outputs
16	V_{CC}	positive supply voltage

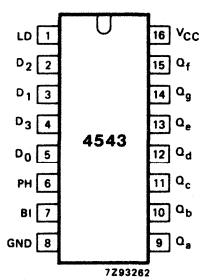


Fig. 1 Pin configuration.

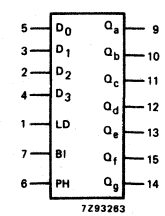


Fig. 2 Logic symbol.

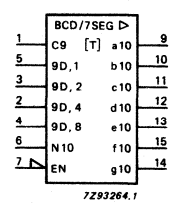


Fig. 3 IEC logic symbol.

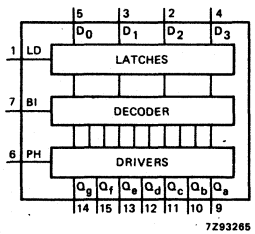


Fig. 4 Functional diagram.

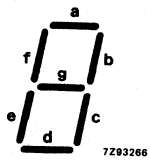


Fig. 5 Segment designation.

APPLICATIONS

- **Driving LCD displays**
- **Driving fluorescent displays**
- **Driving incandescent displays**
- **Driving gas discharge displays**

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH*	D_3	D_2	D_1	D_0	Q_a	Q_b	Q_c	Q_d	Q_e	Q_f	Q_g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

* For liquid crystal displays, apply a square-wave to PH.

** Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level
L = LOW voltage level
X = don't care

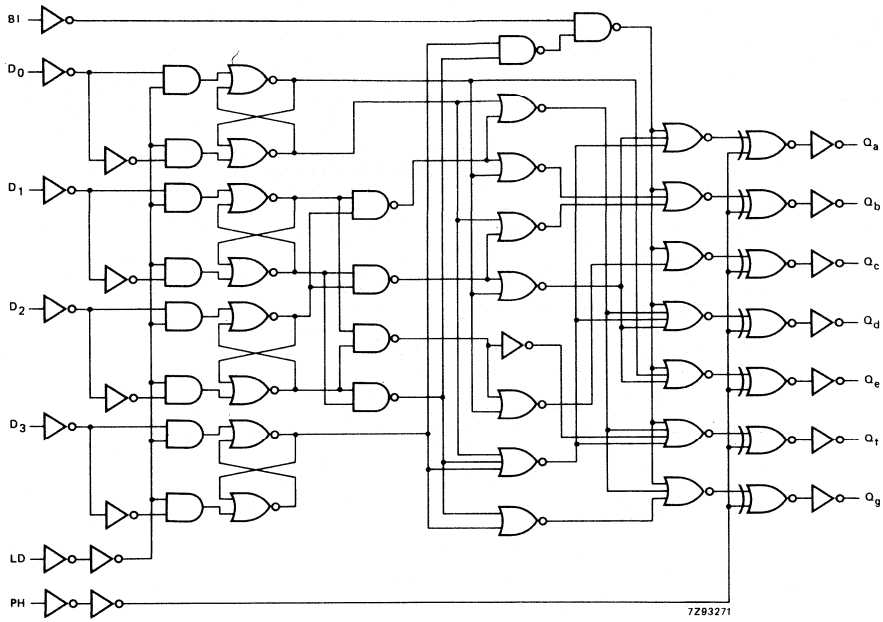


Fig. 6 Logic diagram.

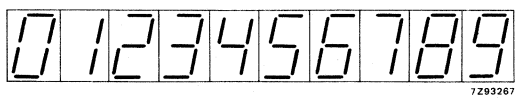


Fig. 7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
For RATINGS see chapter "HCMOS family characteristics", section "Family specifications", standard outputs.

DC CHARACTERISTICS FOR 74HC

Output capability: non-standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.7 1.8 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48	0.15 0.16		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 1.0$ mA $-I_O = 1.3$ mA
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 1.0$ mA $I_O = 1.3$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		91 33 26	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n		102 37 30	370 74 63		465 93 79		555 111 94	ns	2.0 4.5 6.0	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n		66 24 19	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 14
t_{PHL}/t_{PLH}	propagation delay PH to Q_n		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	
t_{THL}/t_{TLH}	output transition time		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	35 7 6	11 4 3		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 13
t_{su}	set-up time D_n to LD	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 15
t_h	hold time D_n to LD	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 15

DC CHARACTERISTICS FOR 74HCT

Output capability: non-standard
I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 1.0$ mA
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 1.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_0, D_1, D_2	1.00
D_3	0.50
$\overline{BI}$	0.50
$\overline{LD}$	1.50
PH	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		38	80		100		120	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay LD to Q_n		36	68		85		102	ns	4.5	Fig. 13
t_{PHL}/t_{PLH}	propagation delay BI to Q_n		32	66		83		99	ns	4.5	Fig. 14
t_{PHL}/t_{PLH}	propagation delay PH to Q_n		24	66		83		99	ns	4.5	
t_{THL}/t_{TLH}	output transition time		23	50		63		75	ns	4.5	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	10	4		13		15		ns	4.5	Fig. 13
t_{su}	set-up time D_n to LD	12	4		15		18		ns	4.5	Fig. 15
t_h	hold time D_n to LD	8	2		10		12		ns	4.5	Fig. 15

APPLICATION DIAGRAMS

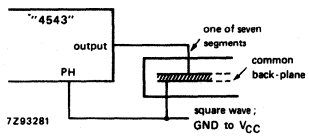


Fig. 8 Connection to liquid crystal (LCD) display readout.

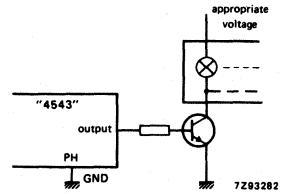


Fig. 9 Connection to incandescent display readout.

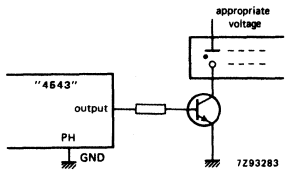


Fig. 10 Connection to gas discharge display readout.

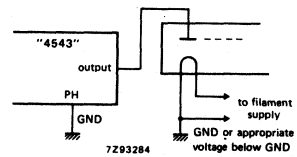


Fig. 11 Connection to fluorescent display readout.

AC WAVEFORMS

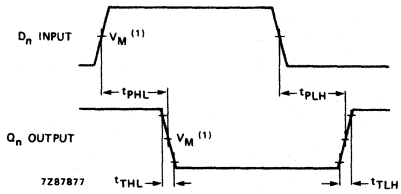


Fig. 12 Waveforms showing the address input (D_n) to output (Q_n) propagation delays and the output transition times.

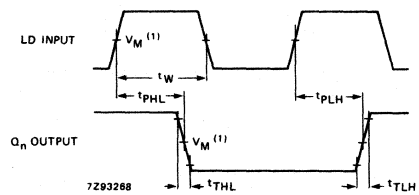


Fig. 13 Waveforms showing the latch disable input (LD) to output (Q_n) propagation delays and the output transition times.

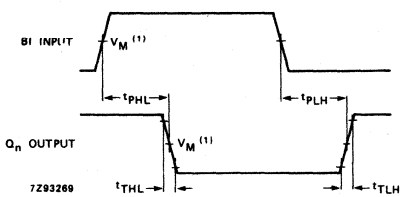


Fig. 14 Waveforms showing the blanking (BI) to output (Q_n) propagation delays and the output transition times.

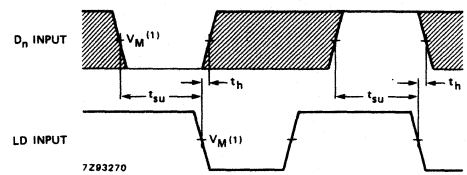


Fig. 15 Waveforms showing the address (D_n) to latch disable (LD) input set-up and hold times.

Note to Fig. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D_A to D_D), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (O_a to O_g).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

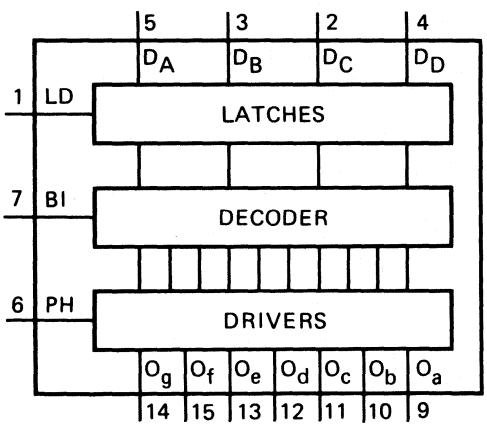


Fig. 1 Functional diagram.

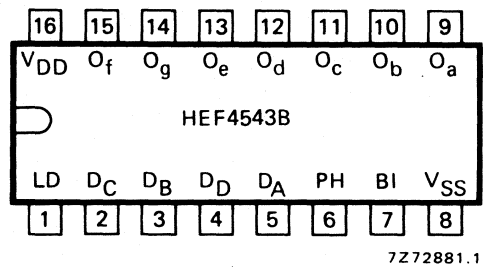


Fig. 2 Pinning diagram.

HEF4543BP : 16-lead-DIL; plastic (SOT-38Z).
HEF4543BD: 16-lead-DIL; ceramic (cerdip) (SOT-74).
HEF4543BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_A to D_D	address (data) inputs
PH	phase input (active HIGH)
BI	blanking input (active HIGH)
LD	latch disable input (active HIGH)
O_a to O_g	segment outputs

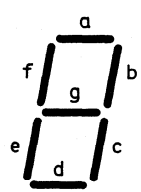


Fig. 3 Segment designation.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

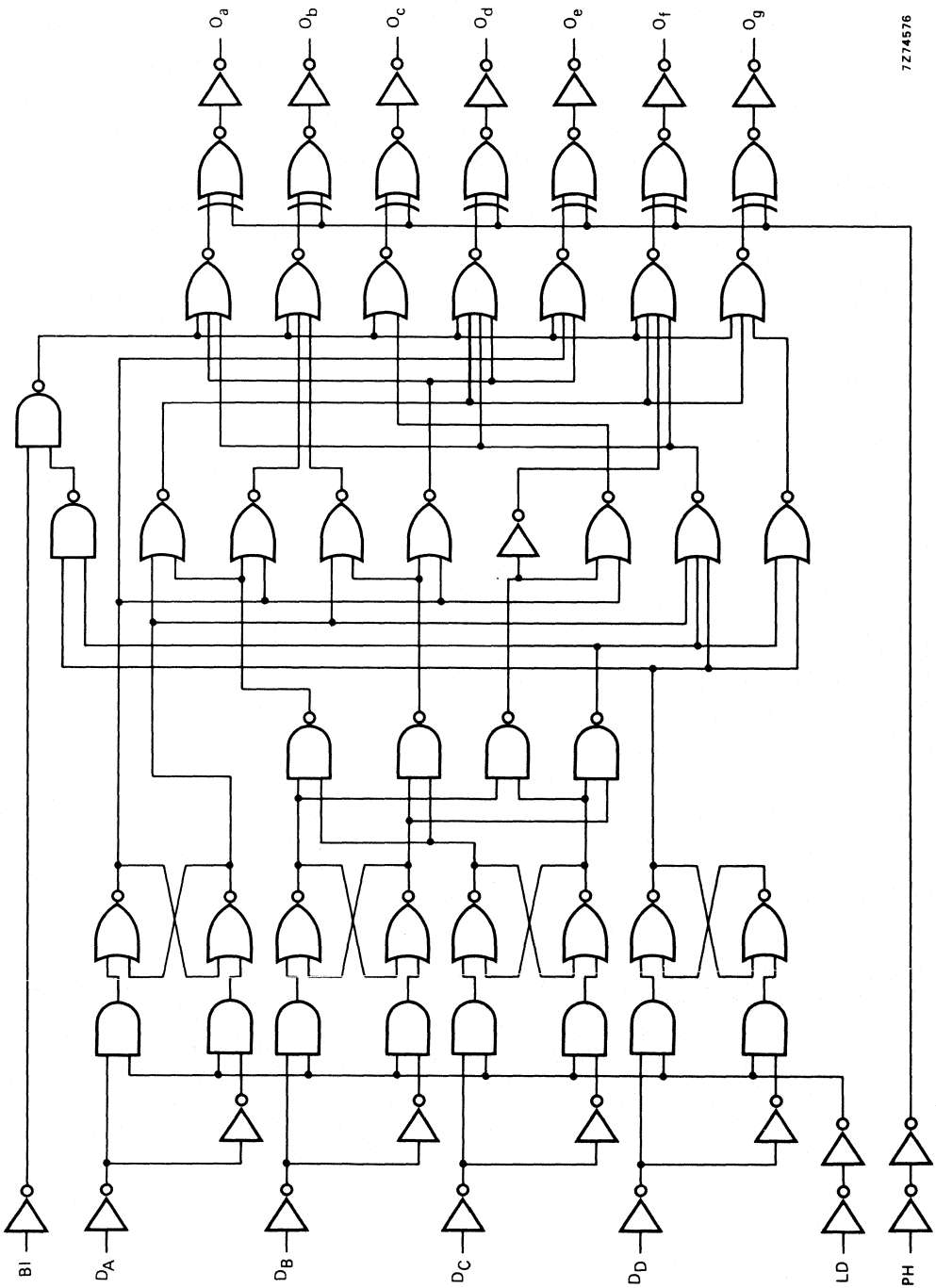


Fig. 4 Logic diagram.

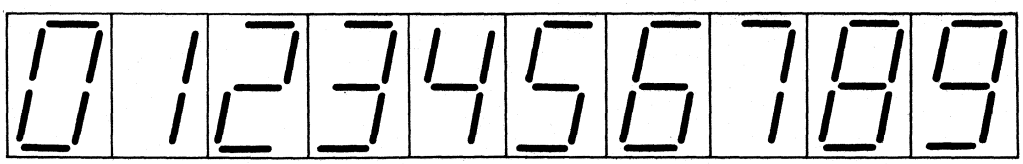
FUNCTION TABLE

inputs							outputs							
LD	BI	PH *	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				* *				* *
as above		H	as above				inverse of above							as above

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* For liquid crystal displays, apply a square-wave to PH.
For common cathode LED displays, select PH = LOW.
For common anode LED displays, select PH = HIGH.

** Depends upon the BCD-code previously applied when LD = HIGH.



7Z72882

Fig. 5 Display.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$D_n \rightarrow O_n$	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
$LD \rightarrow O_n$	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$BI \rightarrow O_n$	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	54 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum LD	5		60	30		ns	
pulse width; HIGH	10	t_{WLDH}	30	15		ns	
	15		20	10		ns	
Set-up time	5		40	20		ns	
$D_n \rightarrow LD$	10	t_{su}	20	5		ns	
	15		15	0		ns	
Hold time	5		0	−15		ns	
$D_n \rightarrow LD$	10	t_{hold}	15	0		ns	
	15		20	5		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	10400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	33000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

APPLICATION INFORMATION

Some examples of applications for the HEF4543B are:

- Driving LCD displays.
- Driving LED displays.
- Driving fluorescent displays
- Driving incandescent displays.
- Driving gas discharge displays.

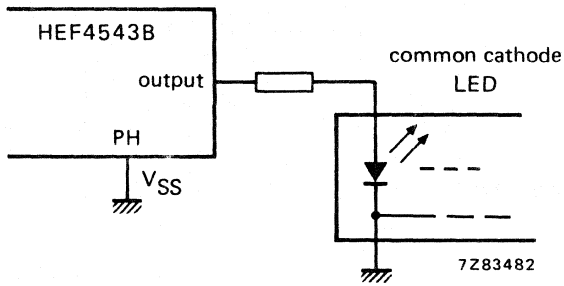


Fig. 6 Connection to common cathode LED display readout.

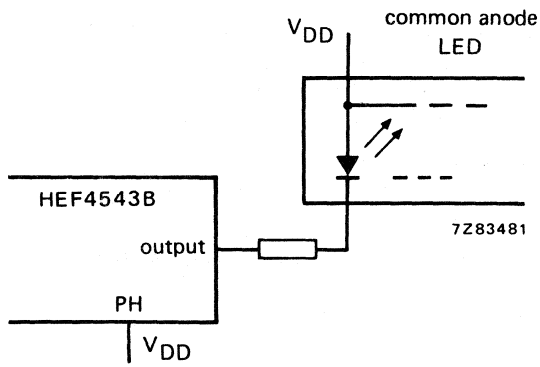


Fig. 7 Connection to common anode LED display readout.

Note to Figs 6 and 7: bipolar transistors may be added for gain where $V_{DD} \leqslant 10$ V or $I_{out} \geqslant 10$ mA.

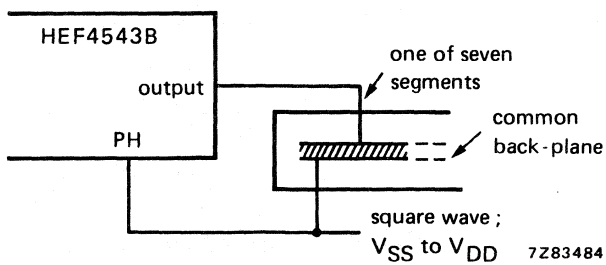


Fig. 8 Connection to liquid crystal (LCD) display readout.

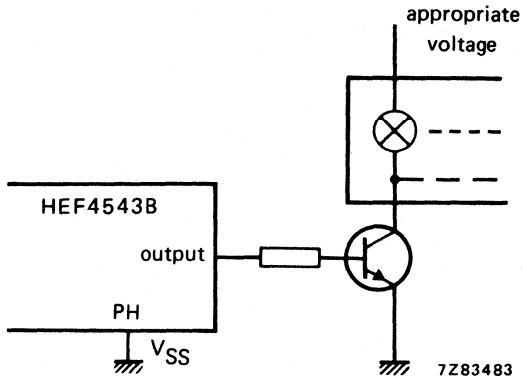


Fig. 9 Connection to incandescent display readout.

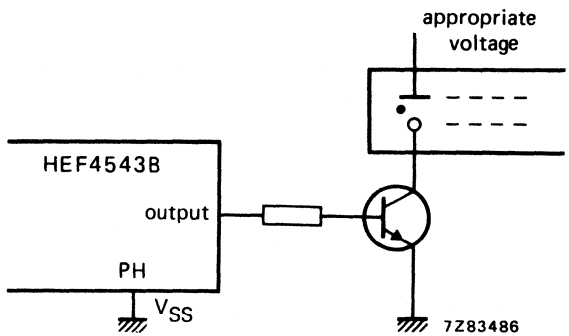


Fig. 10 Connection to gas discharge display readout.

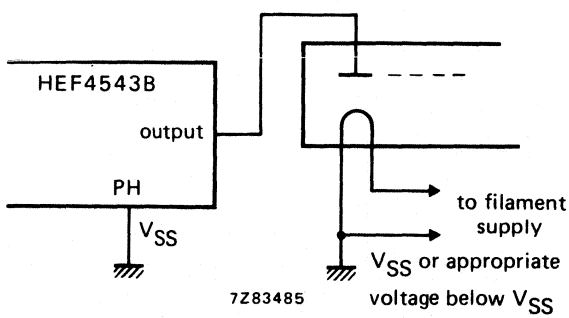


Fig. 11 Connection to fluorescent display readout.

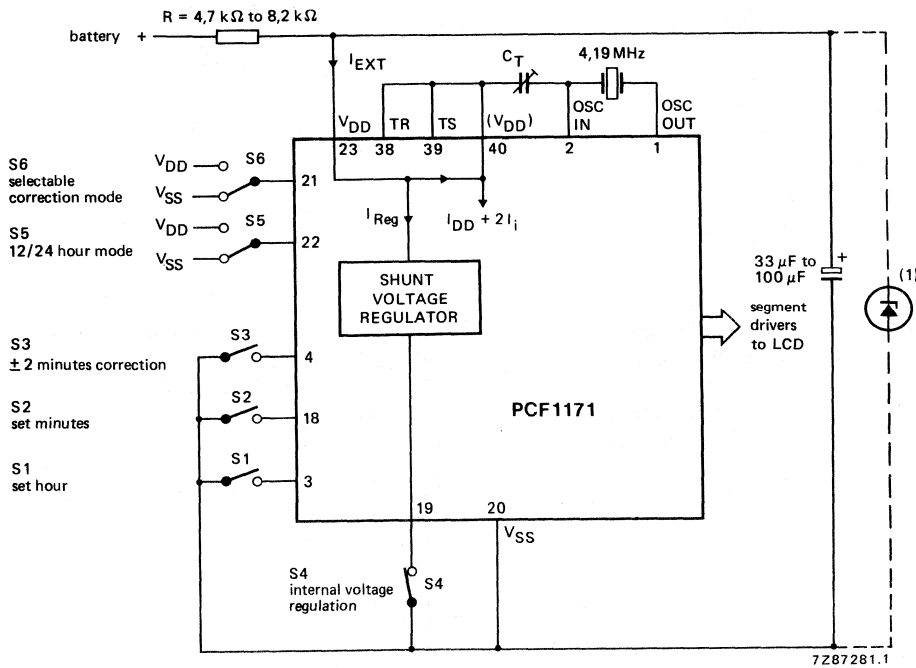
4-DIGIT LCD CAR CLOCK

GENERAL DESCRIPTION

The PCF1171 is a single chip, 4,19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½ or 4-digit liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. A bonding option allows the selection of 12-hour or 24-hour display mode. The circuit is battery operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

Features

- Driving standard 3½ or a 4-digit LCD
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4,19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature range −40 to +85 °C
- 40-lead plastic mini-pack (VSO-40)



(1) Only needed if internal regulation is disconnected.

Fig. 1 Typical application diagram.

Note: From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

PACKAGES OUTLINES

PCF1171BT: 40-lead mini-pack; plastic (VSO-40; SOT-158B).
PCF1171U : uncased chip in tray.

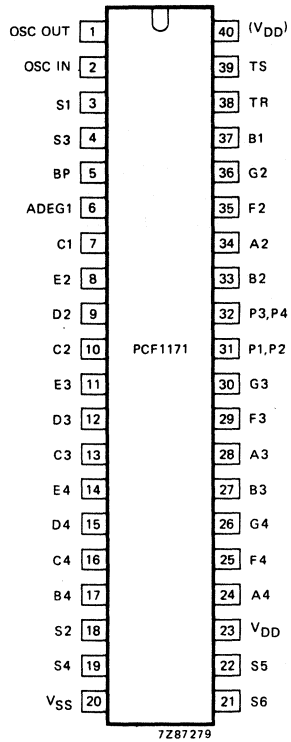


Fig. 2 Pinning diagram.

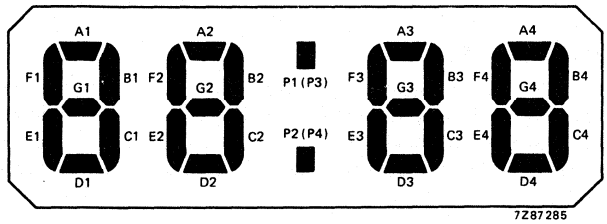


Fig. 3 Segment designation of LCD.

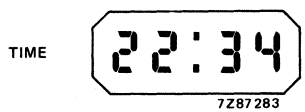


Fig. 4 Display mode.

PINNING

1	OSC OUT	oscillator output
2	OSC IN	oscillator input
3	S1	set hour
4	S3	± 2 minute correction
5	BP	64 Hz backplane driver (common of LCD)
6	ADEG1	segment drivers
7	C1	
8	E2	
9	D2	
10	C2	
11	E3	
12	D3	
13	C3	
14	E4	
15	D4	
16	C4	
17	B4	
18	S2	set minutes
19	S4	internal voltage regulation
20	V_{SS}	negative supply
21	S6	selectable correction mode
22	S5	12/24-hour mode
23	V_{DD}	positive supply
24	A4	segment drivers
25	F4	
26	G4	
27	B3	
28	A3	
29	F3	
30	G3	
31	P1, P2	colon flashing
32	P3, P4	colon static
33	B2	segment drivers
34	A2	
35	F2	
36	G2	
37	B1	
38	TR	test reset; connect to (V_{DD})
39	TS	test speed-up; connect to (V_{DD})
40	(V_{DD})	positive supply for test and oscillator inputs

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Switch S1

Set hours, S6 selects mode of correction.

Switch S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

Switches S1 and S2

Segment test: If S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00 in the 12-hour mode or 0 : 00 in the 24-hour mode.

Switch options

Switch S3

Time correction ± 2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

Switch S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open; the circuit has to be supplied with an externally regulated voltage.

Switch S5

12-hour display mode: S5 is connected to V_{DD} for 12-hour operation.
24-hour display mode: S5 is connected to V_{SS} for 24-hour operation.

Switch S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65 536. In this mode the maximum input frequency is 100 kHz (external generator at OSC_{IN}). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

Switch functions also operate in the test mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS} with internal regulation disconnected *	V_{DD}	max.	8 V
Voltage range (any pin)	V_{n-20}	V_{SS} −0,3 to V_{DD} +0,3	V
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−40 to +85	°C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4,194304 MHz, R_s = 50 Ω, C_L = 12 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (external regulation)	V_{DD}	3	–	6	V
Supply voltage (internal reg. I_{REG} = 1 mA)	V_{DD}	4	5	6	V
Regulation current (with internal regulation)	I_{REG}	0,5	–	5	mA
Current consumption all switches open; without LCD; internal regulation disconnected	I_{DD}	50	250	500	μA
Differential internal impedance at I_{REG} = 1 mA	r_o	–	–	150	Ω
Oscillator (pins 1 and 2)					
start time at $R_{s\,max}$ = 150 Ω	t_{osc}	–	–	200	ms
frequency stability at ΔV_{DD} = 100 mV	$\Delta f/f_{osc}$	–	$0{,}2 \times 10^{-6}$	1×10^{-6}	
feedback resistance	R_{fb}	0,1	–	1	MΩ
input capacitance	C_i	–	–	9	pF
output capacitance	C_o	19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4) and test inputs, TS, TR (pins 38, 39) output current with inputs connected to to V_{SS}	I_i	50	150	500	μA
debounce time	t_d	32	–	150	ms
Segment driver output resistance at ± I_L = 50 μA	R_S	–	1	2,5	kΩ
Backplane driver output resistance at ± I_L = 250 μA	R_{BP}	–	0,2	0,5	kΩ
Backplane driver output frequency	f_{BP}	–	64	–	Hz
LCD d.c. offset voltage at R_L = 200 kΩ; C_L = 1 nF		–	–	±50	mV

Notes to characteristics

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$ (+ LCD current).
2. For correct operation of the oscillator: $V_{DD} \geqslant 3$ V.

* Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

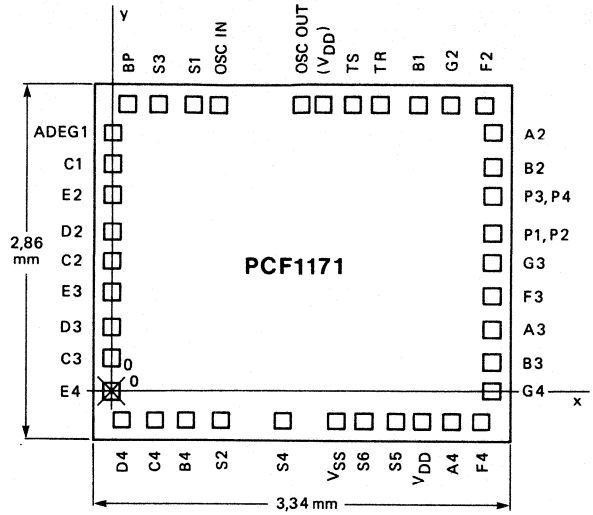


Fig. 5 Bonding pad locations; 40 terminals.

Bonding pad dimensions 100 μm x 100 μm
Chip area = 9,55 mm^2

Table 1 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the pad E4, see Fig. 5.

pad	x	y	pad	x	y
OSC OUT	1510	2330	S6	2040	−230
OSC IN	860	2330	S5	2280	−230
S1	640	2330	V_{DD}	2490	−230
S3	370	2330	A4	2710	−230
BP	110	2330	F4	2960	−230
ADEG1	0	2090	G4	3040	10
C1	0	1840	B3	3040	260
E2	0	1570	A3	3040	530
D2	0	1320	F3	3040	780
C2	0	1050	G3	3040	1060
E3	0	800	P1, P2	3040	1310
D3	0	520	P3, P4	3040	1580
C3	0	270	B2	3040	1830
E4	0	0	A2	3040	2100
D4	80	−230	F2	2970	2300
C4	350	−230	G2	2700	2330
B4	600	−230	B1	2450	2330
S2	890	−230	TR	2160	2330
S4	1380	−230	TS	1930	2330
V_{SS}	1820	−230	V_{DD}	1700	2330
Chip corner max. value	−160	−160			

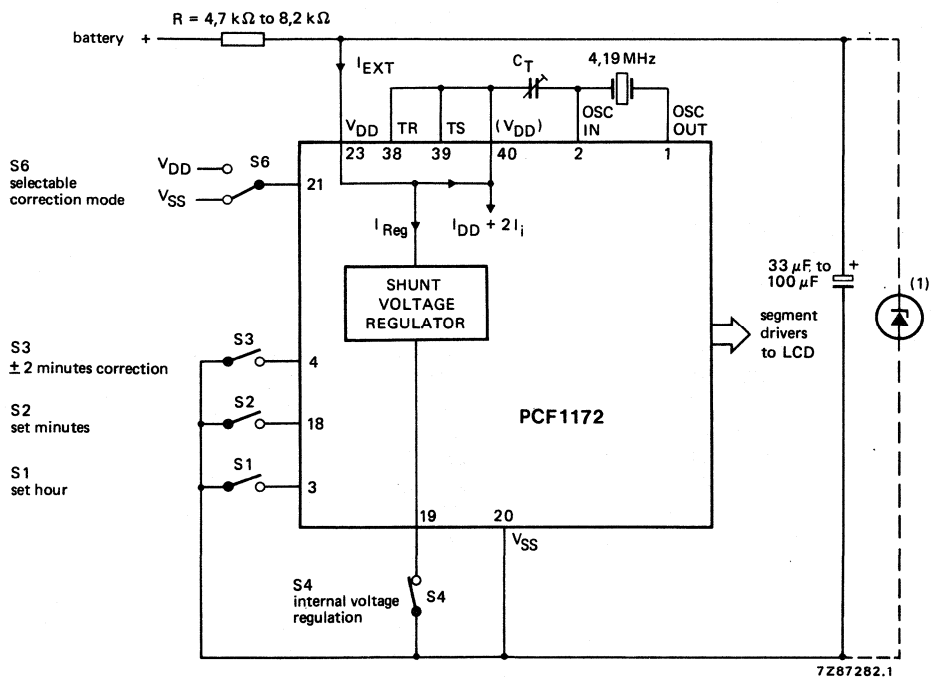
3½-DIGIT LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1172 is a single chip, 4,19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½-digit liquid crystal display (LCD) with AM and PM indicators. Two single-pole, single-throw switches accomplish all time setting functions. The circuit is battery operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

Features

- Driving standard 3½-digit LCD with AM and PM indicators
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4,19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature range −40 to +85 °C
- 40-lead plastic-mini pack (VSO-40)



(1) Only needed if internal regulation is disconnected.

Fig. 1 Typical application diagram.

Note: from pin 2 (OSC IN) to any other pin, the stray capacitance should not exceed 2 pF.

PACKAGE OUTLINES

PCF1172BT: 40-lead mini-pack; plastic (VSO-40; SOT-158B).
PCF1172U : uncased chip in tray.

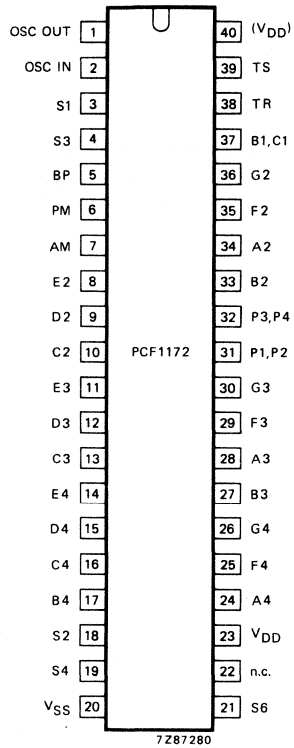


Fig. 2 Pinning diagram.

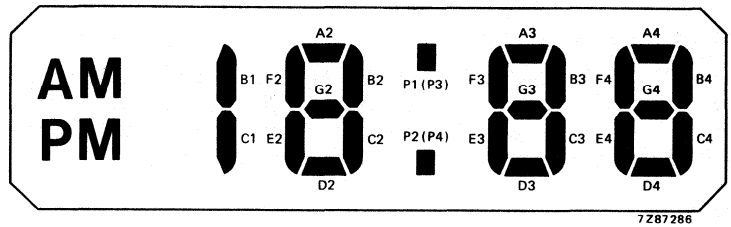


Fig. 3 Segment designation of LCD.

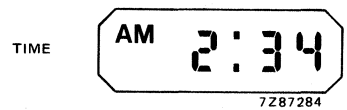


Fig. 4 12-hour display mode.

PINNING

1	OSC OUT	oscillator output
2	OSC IN	oscillator input
3	S1	set hour
4	S3	± 2 minute correction
5	BP	64 Hz backplane driver (common of LCD)
6	PM	segment outputs for PM/AM annunciators
7	AM	
8	E2	segment drivers
9	D2	
10	C2	
11	E3	
12	D3	
13	C3	
14	E4	
15	D4	
16	C4	
17	B4	
18	S2	set minutes
19	S4	internal voltage regulation
20	V_{SS}	negative supply
21	S6	selectable correction mode
22	n.c.	not connected
23	V_{DD}	positive supply
24	A4	segment drivers
25	F4	
26	G4	
27	B3	
28	A3	
29	F3	
30	G3	
31	P1, P2	colon flashing
32	P3, P4	colon static
33	B2	segment drivers
34	A2	
35	F2	
36	G2	
37	B1, C1	
38	TR	test reset; connect to (V_{DD})
39	TS	test speed-up; connect to (V_{DD})
40	(V_{DD})	positive supply for test and oscillator inputs

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Switch S1

Set hours, S6 selects mode of correction.

Switch S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

Switches S1 and S2

Segment test: If S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00.

Switch options

Switch S3

Time correction ± 2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

Switch S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open; the circuit has to be supplied with an externally regulated voltage.

Switch S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65536. In this mode the maximum input frequency is 100 kHz (external generator at OSC_{IN}). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.
Switch functions also operate in the test mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}			
with internal regulation disconnected*	V_{DD}	max.	8 V
Voltage range (any pin)	$V_{n\text{-}20}$	V_{SS} − 0,3 to V_{DD} + 0,3	V
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−40 to +85	°C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4,194304 MHz, R_s = 50 Ω, C_L = 12 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (external regulation)	V_{DD}	3	–	6	V
Supply voltage (internal regulation I_{REG}=1 mA)	V_{DD}	4	5	6	V
Regulation current (with internal regulation)	I_{REG}	0,5	–	5	mA
Current consumption all switches open; without LCD; internal regulation disconnected	I_{DD}	50	250	500	μA
Differential internal impedance at I_{REG} = 1 mA	r_o	–	–	150	Ω
Oscillator (pins 1 and 2)					
start time at $R_{s\,max}$ = 150 Ω	t_{osc}	–	–	200	ms
frequency stability at ΔV_{DD} = 100 mV	$\Delta f/f_{osc}$	–	$0{,}2 \times 10^{-6}$	1×10^{-6}	
feedback resistance	R_{fb}	0,1	–	1	MΩ
input capacitance	C_i	–	–	9	pF
output capacitance	C_o	19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4)					
input current with inputs connected to V_{SS}	I_i	50	150	500	μA
debounce time	t_d	32	–	150	ms
Segment driver output resistance at ± I_L = 50 μA	R_S	–	1	2,5	kΩ
Backplane driver output resistance at ± I_L = 250 μA	R_{BP}	–	0,2	0,5	kΩ
Backplane driver output frequency	f_{BP}	–	64	–	Hz
LCD d.c. offset voltage at R_L = 200 kΩ; C_L = 1 nF		–	–	±50	mV

Notes to characteristics

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$.
2. For correct operation of the oscillator: $V_{DD} \geqslant 3$ V.

* Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

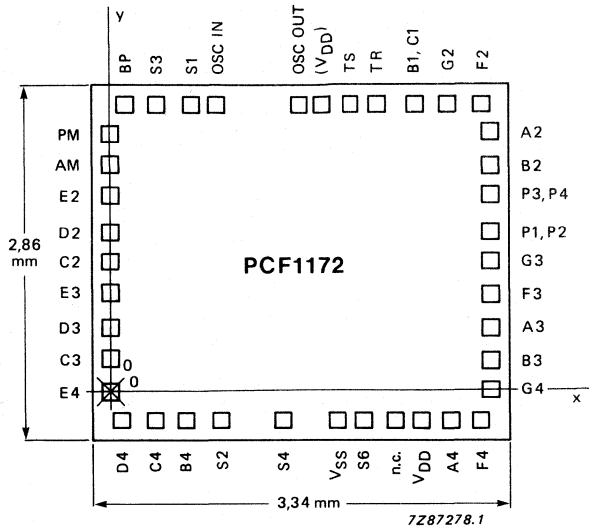


Fig. 5 Bonding pad locations; 40 terminals.

n.c.: not connected
Bonding pad dimensions 100 μm x 100 μm
Chip area = 9,55 mm^2

Table 1 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the pad E4, see Fig. 5.

pad	x	y	pad	x	y
OSC OUT	1510	2330	S6	2040	−230
OSC IN	860	2330	n.c.	2280	−230
S1	640	2330	V_{DD}	2490	−230
S3	370	2330	A4	2710	−230
BP	110	2330	F4	2960	−230
PM	0	2090	G4	3040	10
AM	0	1840	B3	3040	260
E2	0	1570	A3	3040	530
D2	0	1320	F3	3040	780
C2	0	1050	G3	3040	1060
E3	0	800	P1, P2	3040	1310
D3	0	520	P3, P4	3040	1580
C3	0	270	B2	3040	1830
E4	0	0	A2	3040	2100
D4	80	−230	F2	2970	2300
C4	350	−230	G2	2700	2330
B4	600	−230	B1, C1	2450	2330
S2	890	−230	TR	2160	2330
S4	1380	−230	TS	1930	2330
V_{SS}	1820	−230	V_{DD}	1700	2330
Chip corner max. value	−160	−160			

4-DIGIT STATIC-LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1174 is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit static liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery operated via the internal voltage regulator and an external resistor.

Features

- Internal voltage regulator is electrically programmable for various LCD voltages
- Frequency is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range −40 to + 85 °C
- 40-lead plastic mini-pack (VSO-40)

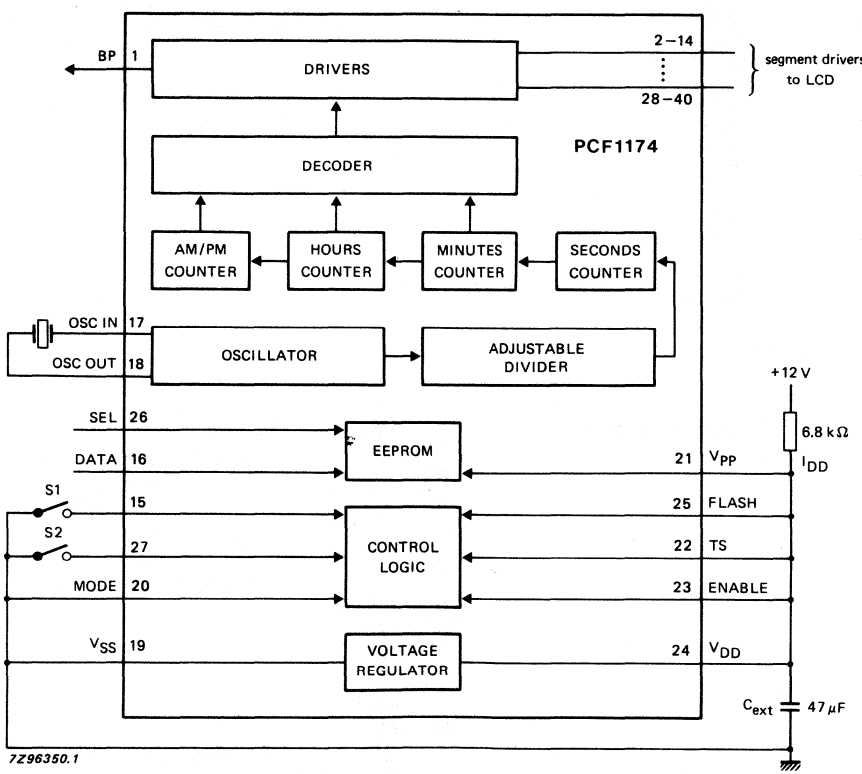


Fig. 1 Typical application diagram.

PACKAGE OUTLINES

PCF1174BT: 40-lead mini-pack; plastic (opposite bent leads) (VSO40; SOT158B).
PCF1174U: uncased chip in tray.

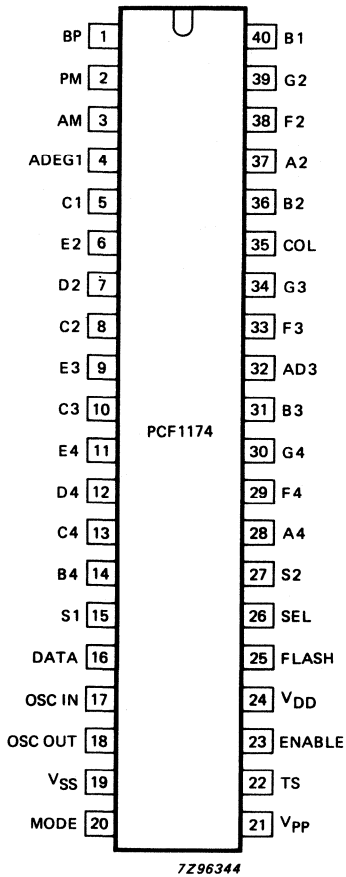


Fig. 2 Pinning diagram.

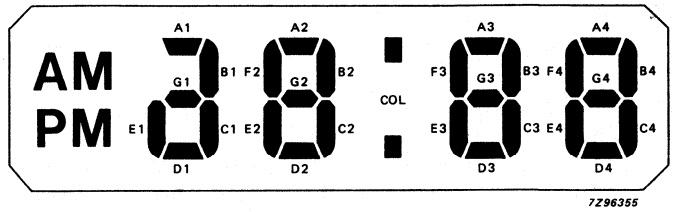
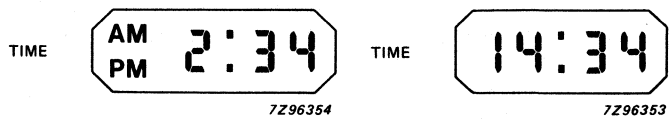


Fig. 3 Segment designation of LCD.



12-hour mode 24-hour mode

Fig. 4 Typical displays.

PINNING

1	BP	backplane output	21	V_{PP}	programming voltage input
2	PM		22	TS	test speed-up mode input
3	AM		23	ENABLE	set enable input for S1 and S2
4	ADEG1		24	V_{DD}	positive supply voltage
5	C1		25	FLASH	colon option input
6	E2		26	SEL	EEPROM select input
7	D2		27	S2	minute adjustment input
8	C2	segment drivers	28	A4	
9	E3		29	F4	
10	C3		30	G4	
11	E4		31	B3	
12	D4		32	AD3	
13	C4		33	F3	
14	B4		34	G3	segment drivers
15	S1	hour adjustment input	35	COL	
16	DATA	EEPROM data input	36	B2	
17	OSC IN	oscillator input	37	A2	
18	OSC OUT	oscillator output	38	F2	
19	V_{SS}	negative supply voltage	39	G2	
20	MODE	12/24 hour mode select input	40	B1	

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. Generation of BP and the output signals are shown in Fig. 5.

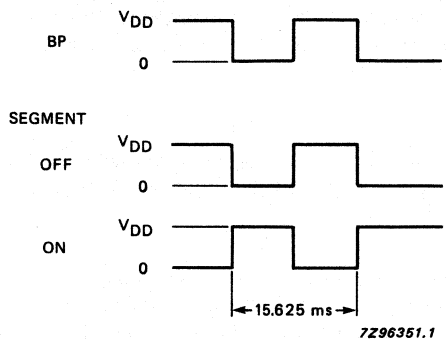


Fig. 5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(rms)} = V_{DD}$
$V_{OFF(rms)} = 0$ V.

LCD voltage

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast:

V_{DD} = 4,5 V at + 25 °C
V_{DD} = 3 to 4 V at + 85 °C.
V_{DD} = 5 to 6 V at −40 °C

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode
0:00 ; 24-hour mode.

Colon

If FLASH is connected to V_{DD}, the colon pulses at 1 Hz. If FLASH is connected to V_{SS}, the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and then continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

Vpp has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of V_{DD} −5 V is applied to Vpp (see Fig. 6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Frequency

Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation + 60 x 10^{-6}) by capacitors at the oscillator input and output.

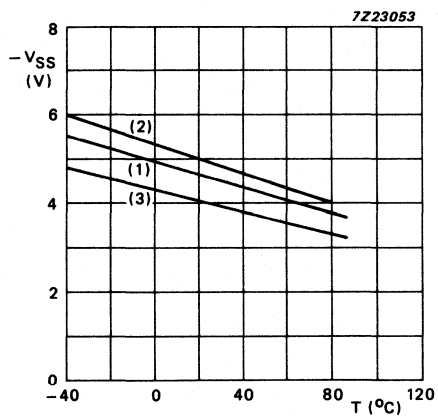
Frequency programming

To enable frequency programming, SEL is set to V_{SS} and a level of V_{DD} −5 V is applied to V_{PP} (see Fig. 7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the highest frequency. Additional pulses (t_L) decrement the frequency in steps as shown in Table 1. Measurement of the backplane period provides a method of checking the new programmed frequency. Once the required frequency is obtained, apply a store pulse (t_W) and release SEL. If the minimum frequency is reached and an additional pulse is applied the frequency will return to the highest programmable value.

Note: PCF1176s are normally delivered with all EEPROM cells programmed to the highest value.

Table 1 Frequency programming ($\Delta t = 7.63\ \mu s$)

frequency deviation $\Delta f/f$ (ppm)	number of pulses n	backplane period (ms)
−3.8	1	15.629
−7.6	2	15.633
−11.4	3	15.636
.	.	.
.	.	.
.	.	.
−117.8	31	15.743



(1) programmed to 4.5 V at 25 °C
(2) programmed to 5.0 V at 25 °C
(3) programmed to 4.0 V at 25 °C

} values within the specified operating range.

Fig. 6 Regulated voltage as a function of temperature (typical).

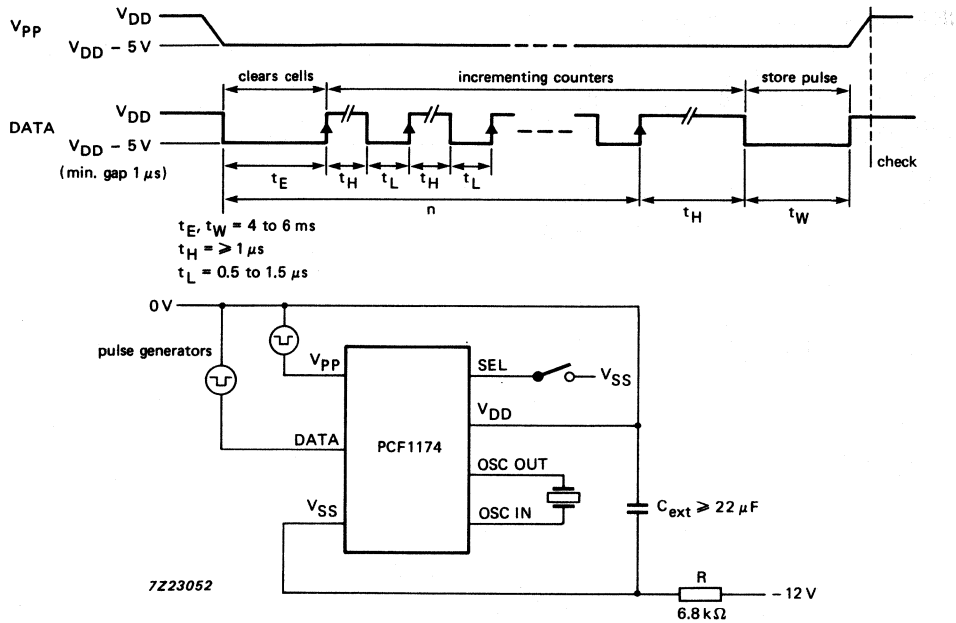


Fig. 7 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	w.r.t V_{SS}	V_{DD}	–	8	V
Supply current	V_{SS} = 0 V; note 1	I_{DD}	–	3	mA
Voltage range	all pins except V_{PP} and DATA	V_I	−0.3	V_{DD} + 0.3	V
Voltage range	pins V_{PP} and DATA	V_I	−3.0	V_{DD} + 0.3	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C

Note to the ratings

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; crystal: frequency = 4.194304 MHz; R_S = 50 Ω, C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

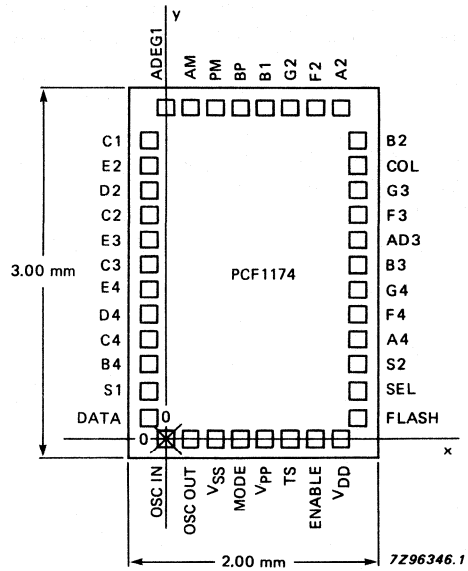
parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	voltage regulator programmed to 4.5 V at 25 °C	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage variation due to temperature		TC	–	−0.35	–	%/K
	V_{DD} = 4.5 V	TC	–	−16	–	mV/K
Supply current	note 1	I_{DD}	700	1000	2000	μA
Capacitance	external capacitor	C_{EXT}	22	47	–	μF
Oscillator						
Start time	$R_{S\ max.}$ = 150 Ω	t_{OSC}	–	–	200	ms
Frequency deviation	nominal n = 0	$\Delta f/f$	0	+ 60	+ 120	10^{-6}
Frequency stability	ΔV_{DD} = 100 mV	$\Delta f/f$	–	–	1	10^{-6}
Input capacitance		C_I	–	16	–	pF
Output capacitance		C_O	–	27	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs						
Pull-up resistance	S1, S2, TS, SEL and DATA	R_O	45	90	180	kΩ
Leakage current	FLASH, ENABLE, MODE	I_{IL}	–	–	2	μA
Debounce time	S1 and S2 only	t_d	30	65	100	ms
Vpp programming voltage						
Output current	$V_{PP} = V_{DD} - 5$ V	I_{O2}	125	–	500	μA
Output current	during programming	I_{O2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{BP}	–	–	3	kΩ
Segment						
Output resistance	± 100 μA	R_{SEG}	–	–	5	kΩ
LCD						
DC offset voltage	200 kΩ/1 nF	V_{DC}	–	–	50	mV

Notes to characteristics

1. A suitable resistor (R) must be selected;
   Example: V_{DD} = 5 V, R max. (12 V − 5 V)/ 700 μA = 10 kΩ
   V_{DD} = 5 V, R typ. (12 V − 5 V)/1000 μA = 7 kΩ (more reserve).

DEVELOPMENT DATA

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6 mm^2
Bonding pad location 100 μm x 100 μm

Fig. 8 Bonding pad locations.

Table 3 Bonding pad dimensions (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left pad (V_{SS}), see Fig. 8.

pad	X	Y	pad	X	Y
BP	600	2676	V_{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V_{DD}	1400	0
C1	−138	2448	FLASH	1538	168
E2	−138	2228	SEL	1538	388
D2	−138	2008	S2	1538	608
C2	−138	1808	A4	1538	808
E3	−138	1608	F4	1538	1008
C3	−138	1408	G4	1538	1208
E4	−138	1208	B3	1538	1408
D4	−138	1008	AD3	1538	1608
C4	−138	808	F3	1538	1808
B4	−138	608	G3	1538	2008
S1	−138	388	COL	1538	2208
DATA	−138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V_{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner (max.)	−300	−160			

4-DIGIT DUPLEX-LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1175 is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery operated via the internal voltage regulator and an external resistor.

Features

- Internal voltage regulator is electrically programmable for various LCD voltages
- Frequency is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range −40 to + 85 °C
- 28-lead plastic mini-pack

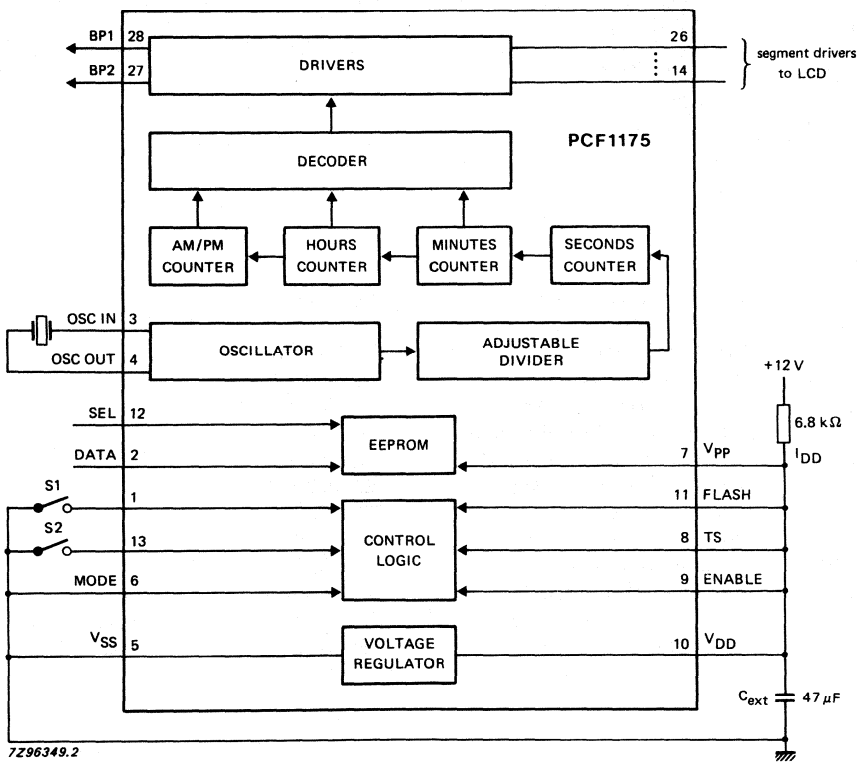


Fig. 1 Typical application diagram.

PACKAGE OUTLINES

PCF1175T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF1175U: uncased chip in tray.
PCF1175U/10: chip-on-film frame carrier (FCC).

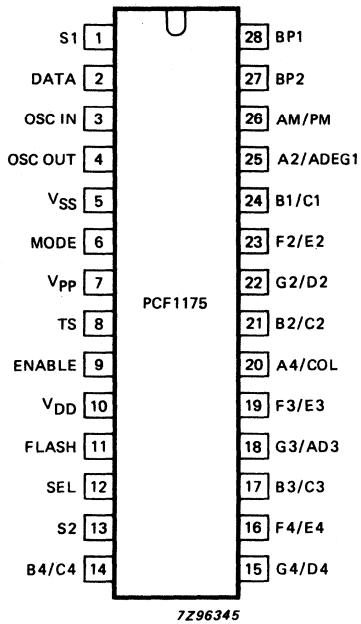


Fig. 2 Pinning diagram.

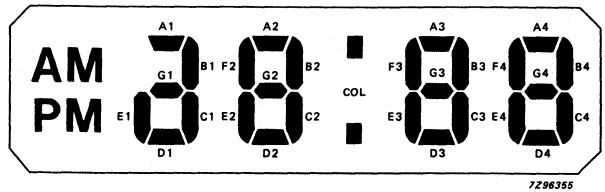


Fig. 3 Segment designation of LCD.

12-hour mode 24-hour mode

Fig. 4 Typical displays.

PINNING

1	S1	hour adjustment input	15	G4/D4	segment drivers
2	DATA	EEPROM data input	16	F4/E4	
3	OSC IN	oscillator input	17	B3/C3	
4	OSC OUT	oscillator output	18	G3/AD3	
5	V_{SS}	negative supply voltage	19	F3/E3	
6	MODE	12/24 hour mode select input	20	A4/COL	
7	V_{PP}	programming voltage input	21	B2/C2	
8	TS	test speed-up mode input	22	G2/D2	
9	ENABLE	enable input (for S1 and S2)	23	F2/E2	
10	V_{DD}	positive supply voltage	24	B1/C1	
11	FLASH	colon option input	25	A2/ADEG1	
12	SEL	EEPROM select input	26	AM/PM	
13	S2	minute adjustment input	27	BP2	backplane 2
14	B4/C4	segment drivers	28	BP1	backplane 1

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig. 5.

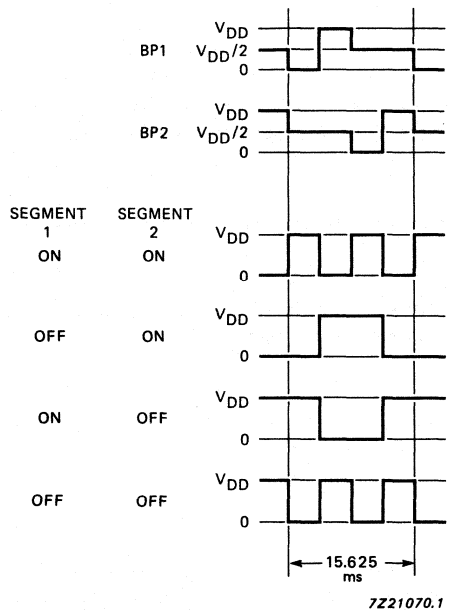


Fig. 5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(rms)} = 0.79\ V_{DD}$
$V_{OFF(rms)} = 0.35\ V_{DD}$

LCD voltage

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast:

V_{DD} = 5 to 6 V at −40 °C
V_{DD} = 4.5 V at + 25 °C
V_{DD} = 3 to 4 V at + 85 °C

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

DEVELOPMENT DATA

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode (MODE connected to V_{DD})
0:00 ; 24-hour mode (MODE connected to V_{SS} or left open-circuit).

Colon

If FLASH is connected to V_{DD}, the colon pulses at 1 Hz. If FLASH is connected to V_{SS}, the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and then continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode.
When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of V_{DD} −5 V is applied to V_{PP} (see Fig. 6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Additional pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Frequency

Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation + 60 x 10^{-6}) by capacitors at the oscillator input and output.

Frequency programming

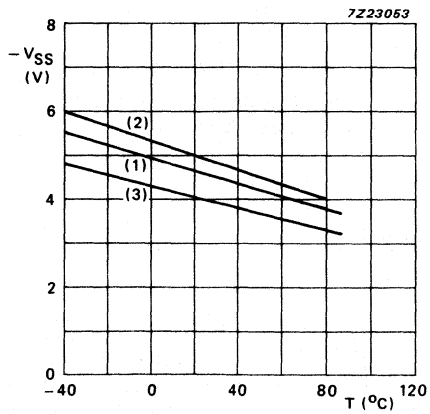
To enable frequency programming, SEL is set to V_{SS} and a level of V_{DD} −5 V is applied to V_{PP} (see Fig. 7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the highest frequency. Additional pulses (t_L) decrement the frequency in steps as shown in Table 1. Measurement of the backplane period provides a method of checking the new programmed frequency. Once the required frequency is obtained, apply a store pulse (t_W) and release SEL. If the minimum frequency is reached and an additional pulse is applied the frequency will return to the highest programmable value.

Note: PCF1175s are normally delivered with all EEPROM cells programmed to the highest value.

Table 1 Frequency programming (Δt = 7.63 μs)

frequency deviation $\Delta f/f$ (ppm)	number of pulses n	backplane period (ms)
−3.8	1	15.633
−7.6	2	15.641
−11.4	3	15.648
.	.	.
.	.	.
−117.8	31	15.861

DEVELOPMENT DATA



(1) programmed to 4.5 V at 25 °C
(2) programmed to 5.0 V at 25 °C
(3) programmed to 4.0 V at 25 °C

} values within the specified operating range

Fig. 6 Regulated voltage as a function of temperature (typical).

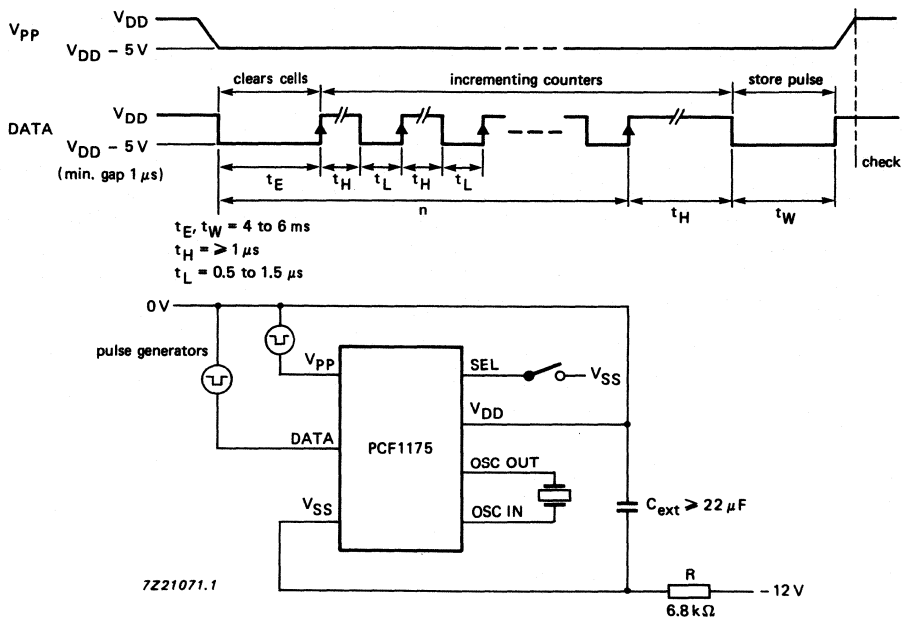


Fig. 7 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	w.r.t V_{SS}	V_{DD}	–	8	V
Supply current	V_{SS} = 0 V; note 1	I_{DD}	–	3	mA
Voltage range	all pins except V_{PP} and DATA	V_I	−0.3	V_{DD} + 0.3	V
Voltage range	pins V_{PP} and DATA	V_I	−3.0	V_{DD} + 0.3	V
Storage temperature range		T_{stg}	−55	+ 125	°C
Operating ambient temperature range		T_{amb}	−40	+ 85	°C

Note to the ratings

1. Connecting the supply voltage with reverse polarity will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; crystal: frequency = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

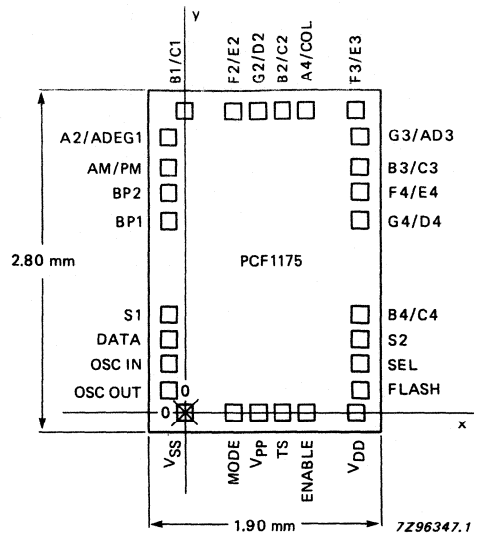
parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	voltage regulator programmed to 4.5 V at 25 °C	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage variation due to temperature		TC	–	−0.35	–	%/K
	V_{DD} = 4.5 V	TC	–	−16	–	mV/K
Supply current	note 1	I_{DD}	700	1000	2000	μA
Capacitance	external capacitor	C_{EXT}	22	47	–	μF
Oscillator						
Start time	$R_{Smax.}$ = 150 Ω	t_{OSC}	–	–	200	ms
Frequency deviation	nominal n = 0	Δf/f	0	+ 60	+ 120	10^{-6}
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	–	1	10^{-6}
Input capacitance		C_I	–	16	–	pF
Output capacitance		C_O	–	27	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs						
Pull-up resistance	S1, S2, TS, SEL and DATA	R_O	45	90	180	kΩ
Leakage current	ENABLE, FLASH	I_{IL}	–	–	2	μA
Pull-up/pull-down resistance	MODE	R_O	150	300	600	kΩ
Debounce time	S1 and S2 only	t_d	30	65	100	ms
Vpp programming voltage						
Output current	Vpp = V_{DD} − 5 V	I_{O2}	125	–	500	μA
Output current	during programming	I_{O2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{BP}	–	–	3	kΩ
Segment						
Output resistance	± 100 μA	R_{SEG}	–	–	5	kΩ
LCD						
DC offset voltage	200 kΩ/1 nF	V_{DC}	–	–	50	mV

Notes to characteristics

1. A suitable external resistor (R) must be selected:

   Example: V_{DD} = 5 V, R max. (12 V − 5 V)/ 700 μA = 10 kΩ
   V_{DD} = 5 V, R typ. (12 V − 5 V)/1000 μA = 7 kΩ (more reserve).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.32 mm^2
Bonding pad location 100 μm x 100 μm

Fig. 8 Bonding pad locations.

Table 3 Bonding pad dimensions (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left pad (V_{SS}), see Fig. 8.

pad	X	Y	pad	X	Y
S1	−138	848	G4/D4	1438	1588
DATA	−138	628	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	400	0	A4/COL	1000	2476
V_{PP}	600	0	B2/C2	800	2476
TS	800	0	G2/D2	600	2476
ENABLE	1000	0	F2/E2	400	2476
V_{DD}	1400	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	838	BP1	−138	1588
chip corner (max.)	−300	−160	−160		

DEVELOPMENT DATA

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the PCF84CXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the "Single-chip 8-bit Microcontrollers user manual".

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} \leqslant V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT-208).

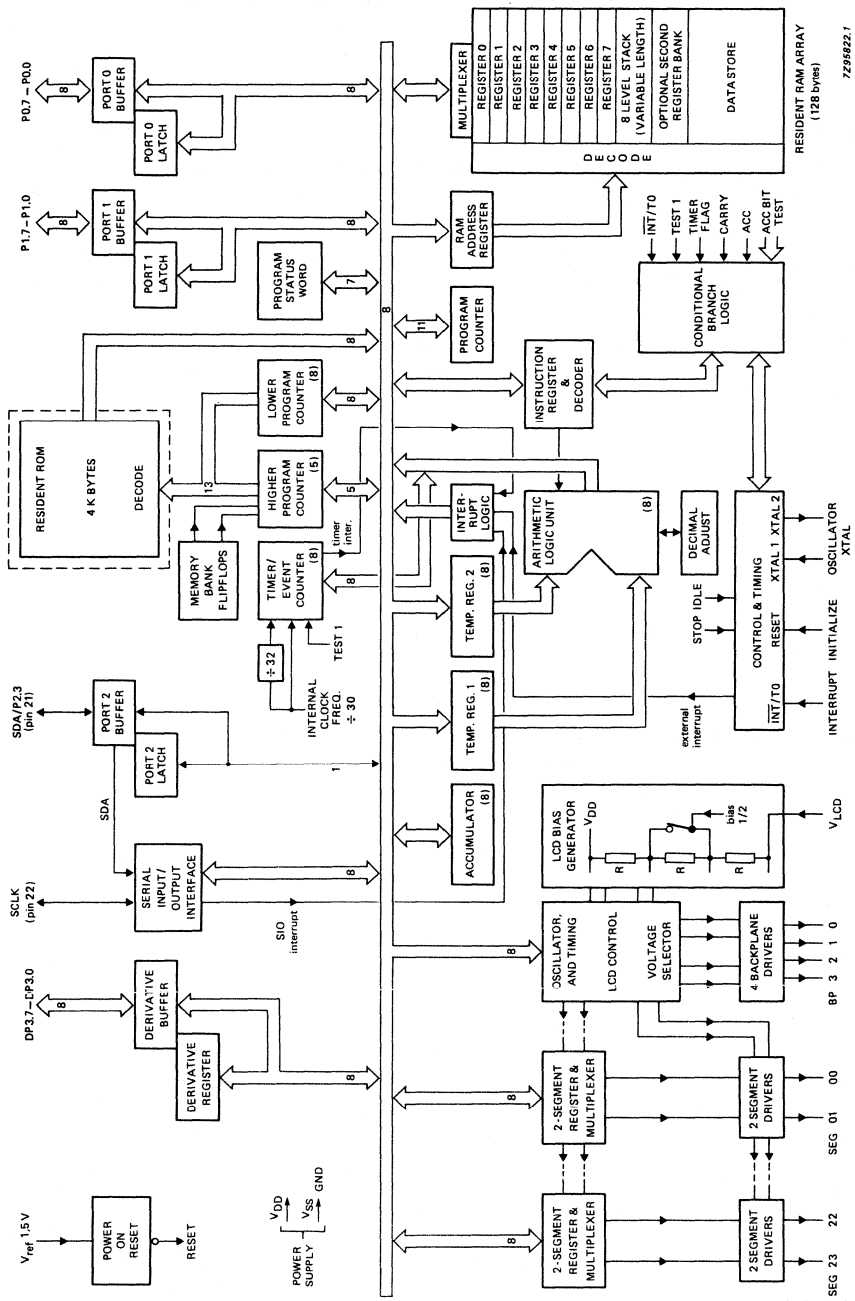


Fig. 1 Block diagram; PCF84C430.

DEVELOPMENT DATA

PINNING

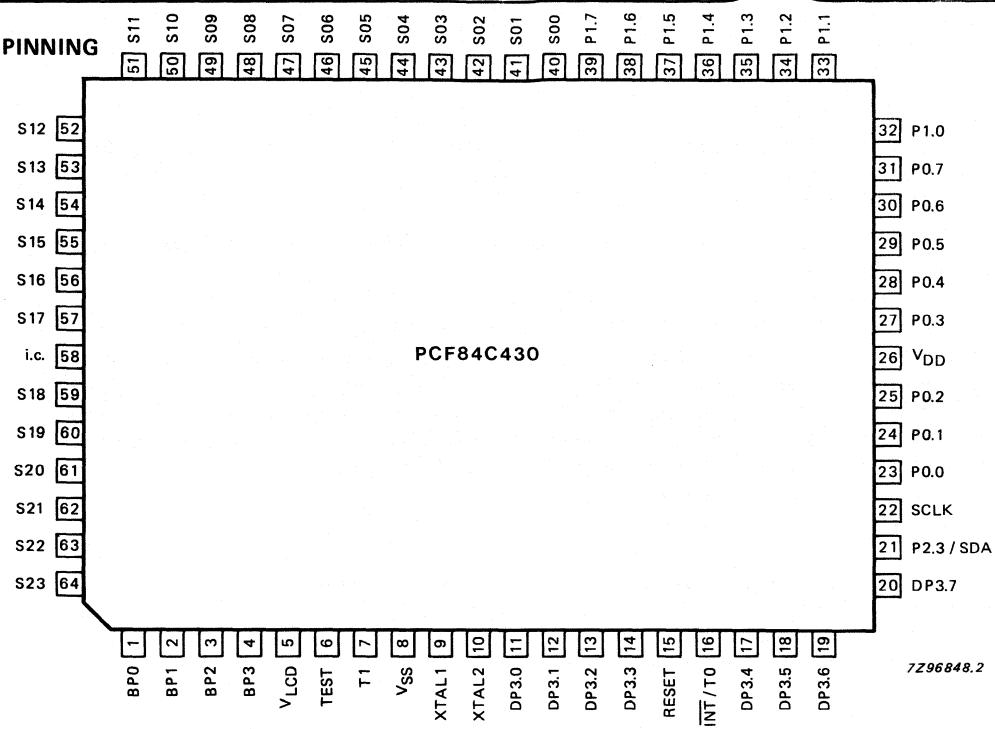


Fig. 2 Pin designation of the PCF84C430.

PIN DESIGNATION

pin	symbol	type	function
1-4	BP0-BP3	O	**LCD:** backplane outputs.
5	V_{LCD}		**LCD:** supply voltage.
6	TEST	I	**Test pin:** to be grounded for normal operation.
7	T1	I	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
8	V_{SS}		**Ground:** circuit earth potential.
9	XTAL1	I	**Oscillator input:** crystal which determines the internal oscillator frequency or the external clock generator.
10	XTAL2	I/O	Connection to other side of timing component.
11-14	DP3.0-DP3.3	I/O	**Derivative port 3:** 8-bit parallel port LSBs.
15	RESET	I/O	**Reset input:** used to initialize the processor (active HIGH), or output of power-on-reset circuit.
16	$\overline{INT}$/T0	I	**Interrupt/Test 0:** external interrupt input (sensitive to negative going edge)/test input; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
17-20	DP3.4-DP3.7	I/O	**Derivative port 3:** 8-bit parallel port MSBs.
21	SDA/P23	I/O	**Serial data:** input/output in serial I/O mode. If not selected as serial data pin, P23 functions as a quasi-bidirectional I/O line.
22	SCLK	I/O	**Serial clock:** bidirectional clock for serial I/O.
23-25 27-31	P0.0-P0.7	I/O	**Port 0:** 8-bit quasi-bidirectional I/O port.
26	V_{DD}		**Power supply:** 2,5 V to 5,5 V.
32-39	P1.0-P1,7	I/O	**Port 1:** 8-bit quasi-bidirectional I/O port.
40-57 59-64	S00-S23	O	**LCD** segment driver outputs.

FUNCTIONAL DESCRIPTION

Program memory

The program memory consists of 4 K bytes, in a read-only memory (ROM).
Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET)
- Location 3; contains the first byte of an external interrupt service subroutine
- Location 5; contains the first byte of a serial I/O and interrupt service subroutine
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 128 bytes, random-access data memory (RAM).
All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

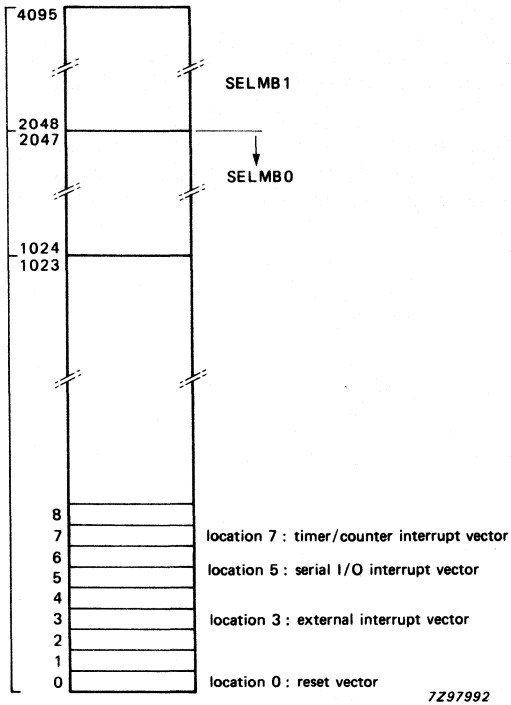


Fig. 3 Program memory map.

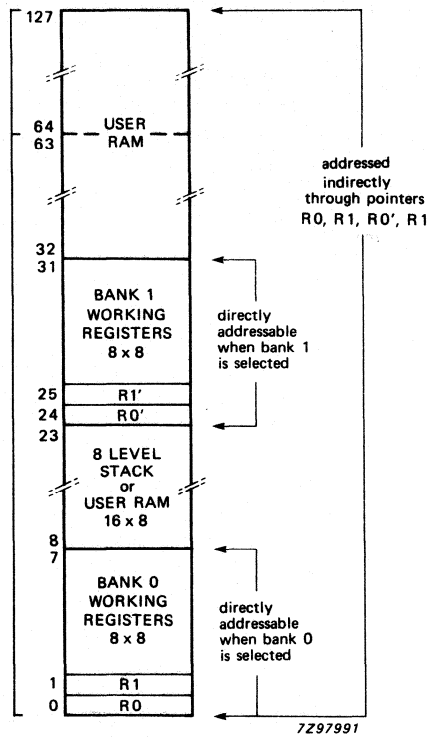


Fig. 4 Data memory map.

DEVELOPMENT DATA

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack (continued)

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

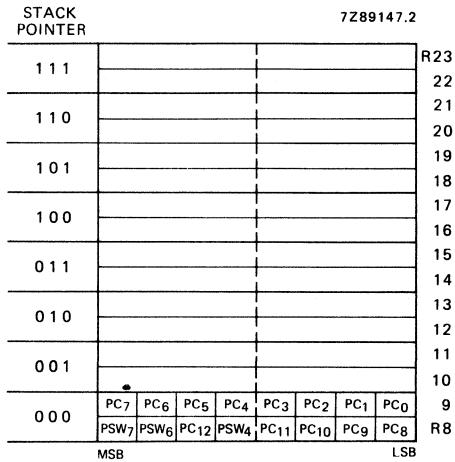


Fig. 5 Program counter stack.

IDLE and STOP modes

Idle mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01 H) the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled, or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

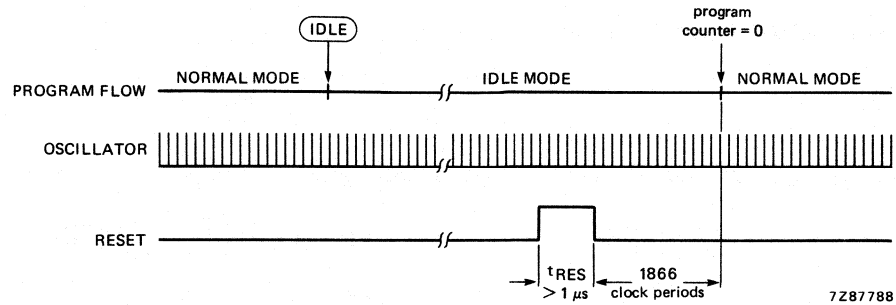


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A HIGH-to-LOW transition on the external interrupt pin ($\overline{INT}$/T0) reactivates the microcontroller. A LOW level applied to $\overline{INT}$/T0 will reactivate the microcontroller only in the STOP mode. Thus, if $\overline{INT}$/T0 was LOW before the microcontroller entered the IDLE mode, it must go HIGH before the microcontroller can be reactivated (see Fig. 7.).

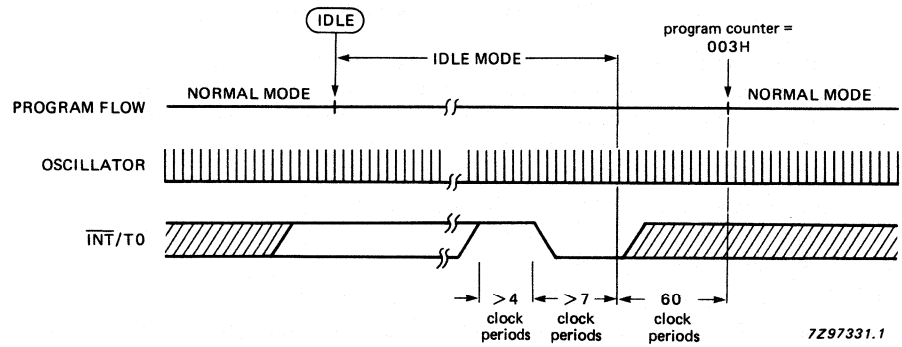


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when $\overline{INT}$/T0 is HIGH for at least 4 CP (clock periods) followed by a LOW for 7 CP. After the initial forced CALL 003 H operation (60 CP) the program continues with the external interrupt service routine. During IDLE mode operation, the address of the instruction immediately following that which caused the processor to enter the IDLE mode is present on the address bus.

STOP mode

The microcontroller enters the STOP mode via the STOP instruction (22H). The oscillator is switched off but internal status of the CPU, RAM contents and the state of I/O ports are unaffected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8). Note: the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

FUNCTIONAL DESCRIPTION (continued)

STOP mode (continued)

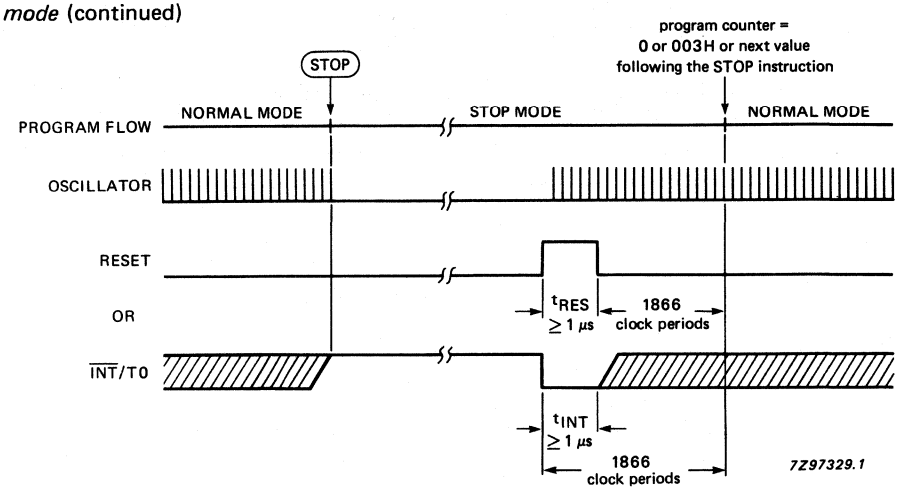


Fig. 8 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin LOW, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a LOW level applied at the $\overline{INT}$/T0 pin.
Note: when leaving the STOP mode via an interrupt, a further instruction in the main program series is executed prior to entering the interrupt routine.

When the $\overline{INT}$/T0 level is active during the STOP instruction then no STOP is executed.

A LOW level on the external interrupt input of at least 1 µs will cause the microcontroller to exit the STOP mode. During the STOP mode, the address of the instruction immediately following the last STOP instruction is present on the address bus.

I/O facilities

The PCF84C430 has 25 quasi-bidirectional I/O lines arranged as:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 8 lines (P1.0 to P1.7)
- Port 2 I/O port of 1 line (SDA/P2.3) active when not selected as serial I/O
- Port 3 a derivative 8-bit parallel port (DP3.0 to DP3.7)

In addition 4 specialized I/O lines are comprised:

- SCLK serial I/O clock line
- SDA/P2.3 serial I/O data line
- $\overline{INT}$/T0 external interrupt and test input. When used as a test input it can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one TTL or CMOS load.

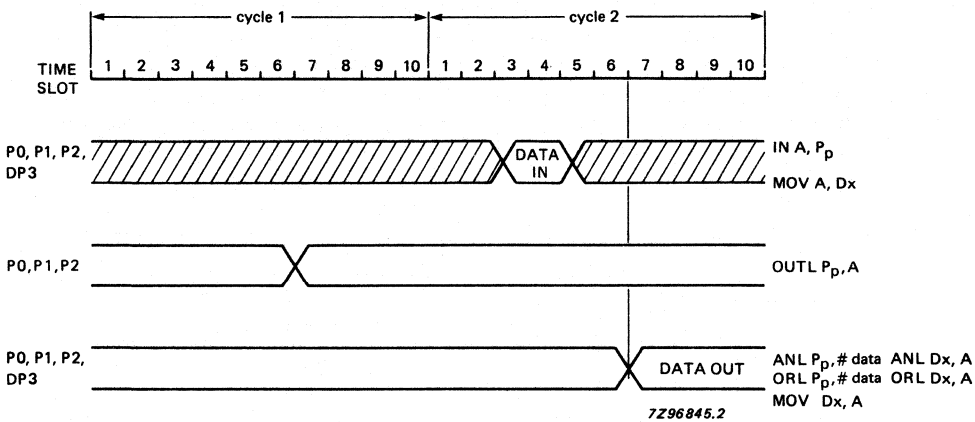


Fig. 9 Shows the timing diagram for all ports using IN, OUTL, ANL and ORL instructions. For the OUTL instruction data changes on time slot 7 of cycle 1. For the MOV, ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

FUNCTIONAL DESCRIPTION (continued)

Parallel ports (continued)

The PCF84C430 family offers the possibility to select individually 24 of the 25 parallel port pins (not P2.3)* from the following mask options:

Option 1 – STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2.
TR2 is only active during 1 clock cycle (Fig. 10).

Option 2 – OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11). When an open drain port is unused it must be connected to V_{SS}.

Option 3 – PUSH-PULL OUTPUT; drive capability of the output is 1,6 mA (min.) at V_{DD} = 5 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 12).
Note: the port latch may be read back using the IN A,pp instruction.

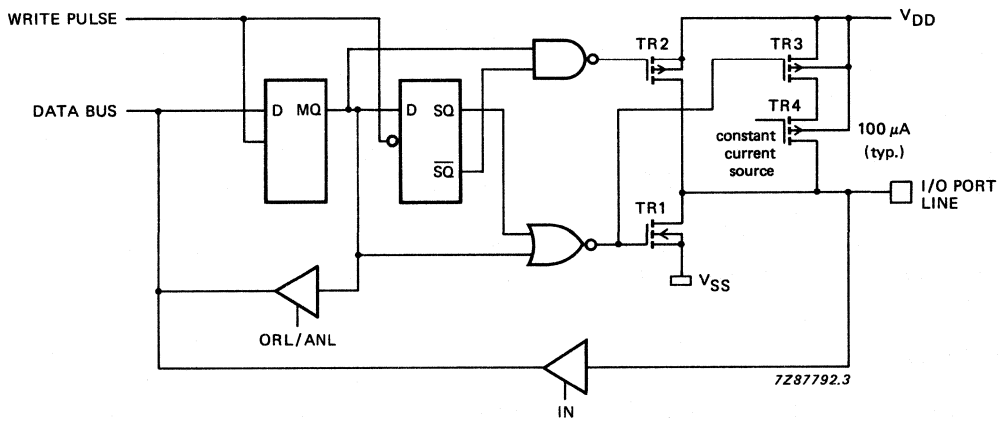


Fig. 10 Standard output with switch pull-up current source.

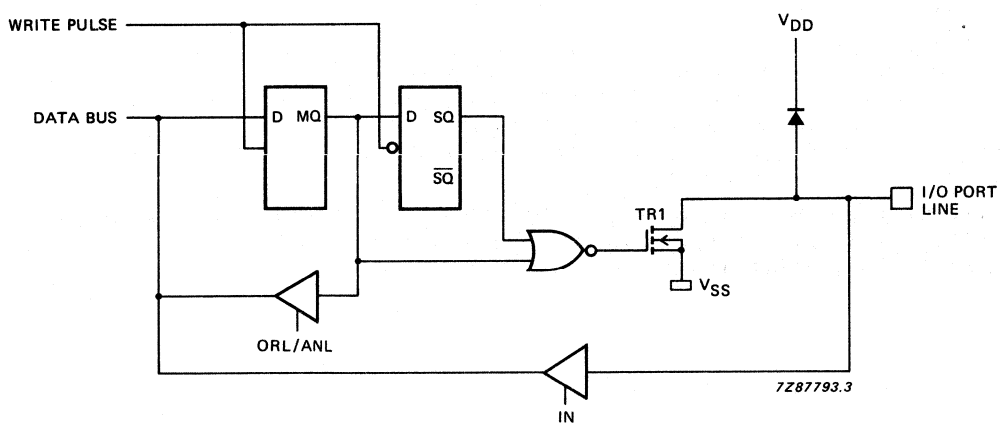


Fig. 11 Open drain output.

* P2.3 is always open drain.

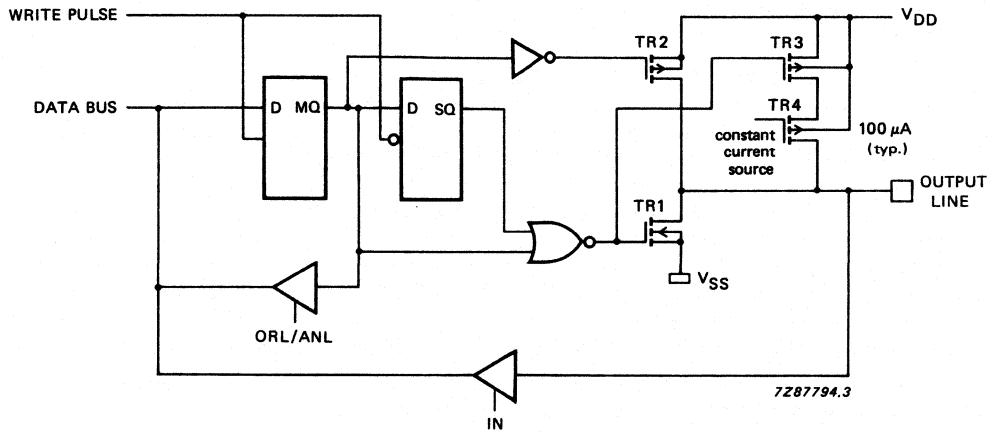


Fig. 12 Push-pull output.

Derivative I/O addresses

For extension of the I/O facilities, instructions MOV A,Dx, MOV Dx,A, ANL Dx,A and ORL Dx,A have been added to the instruction set. The derivative register address is the second byte of the instruction. The address map for the derivative registers is given in Table 1.

Table 1 address map of PCF84C430 derivative registers

Dx	R/W	bits	description
4	R/W	8	PR3; derivative I/O port 3 latch
5	R	8	PR3; derivative I/O port 3 input pins
16	R/W	8	LCDC; LCD control register
17-28	R/W	8	LCDB1-LCDB12; 12 consecutive segment data bytes

Serial I/O (SIO)

The PCF84C430 has an on-chip serial I/O interface that supports I^2C-bus communication. Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCF84C430 only when a complete byte is received. It then reads the data byte in one instruction.

During transmission, the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO) (continued)

The design of the PCF84C430 serial I/O system allows any number of devices from PCF85XX family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically, invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCF84C430 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCF84C430 has finished a serial data transfer.

After a negative-going RESET signal, the first 30 clock pulses of the 1866-pulse initialization phase set P2.3/SDA and SCLK to HIGH. When P2.3/SDA or SCLK are not used they must be connected to V_{SS}.

Serial I/O interface

Figure 13 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 22 (SCLK) while the data line shares pin 21 (SERIAL DATA) with the I/O line P2.3 of port 2. When the serial I/O is enabled, P2.3 is disabled as a parallel port line; (P2.3 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register (SO')

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while status bits can only be read.

MST and TRX (see Table 2)

These bits determine the operating mode of the serial I/O interface.

Table 2 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial Output

The ESO flag enables/disables the serial I/O interface: ESO = 1 enables, ESO = 0 disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O interface (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 154 kHz and 1 kHz (see Table 3).
An asymmetrical clock with a HIGH-to-LOW ratio of 3:1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O.
S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ESO = 0 .

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 3 SIO clock pulse frequency control when using a 6 MHz and a 10 MHz crystal

hexadecimal S20-S24 code	divisor	f_{XTAL} (6 MHz) f_{SCLK} (kHz)▲	f_{XTAL} (10 MHz) f_{SCLK} (kHz)▲
0	not allowed		
1	39	*154	*256
2	45	*133	*222
3	51	*118	*196
4	63	95	*159
5	75	80	*133
6	87	69	*115
7	99	61	*101
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8,9	15
13	771	7,8	13,4
14	963	6,2	10,4
15	1155	5,2	8,7
16	1347	4,5	7,4
17	1539	3,9	6,5
18	1923	3,1	5,2
19	2307	2,6	4,3
1A	2691	2,2	3,7
1B	3075	2,0	3,3
1C	3843	1,6	2,6
1D	4611	1,3	2,2
1E	5379	1,1	1,9
1F	6147	1,0	1,6

DEVELOPMENT DATA

* Not permitted for I^2C operation.

▲ The maximum clock frequency in the I^2C systems is 100 kHz.

FUNCTIONAL DESCRIPTION (continued)

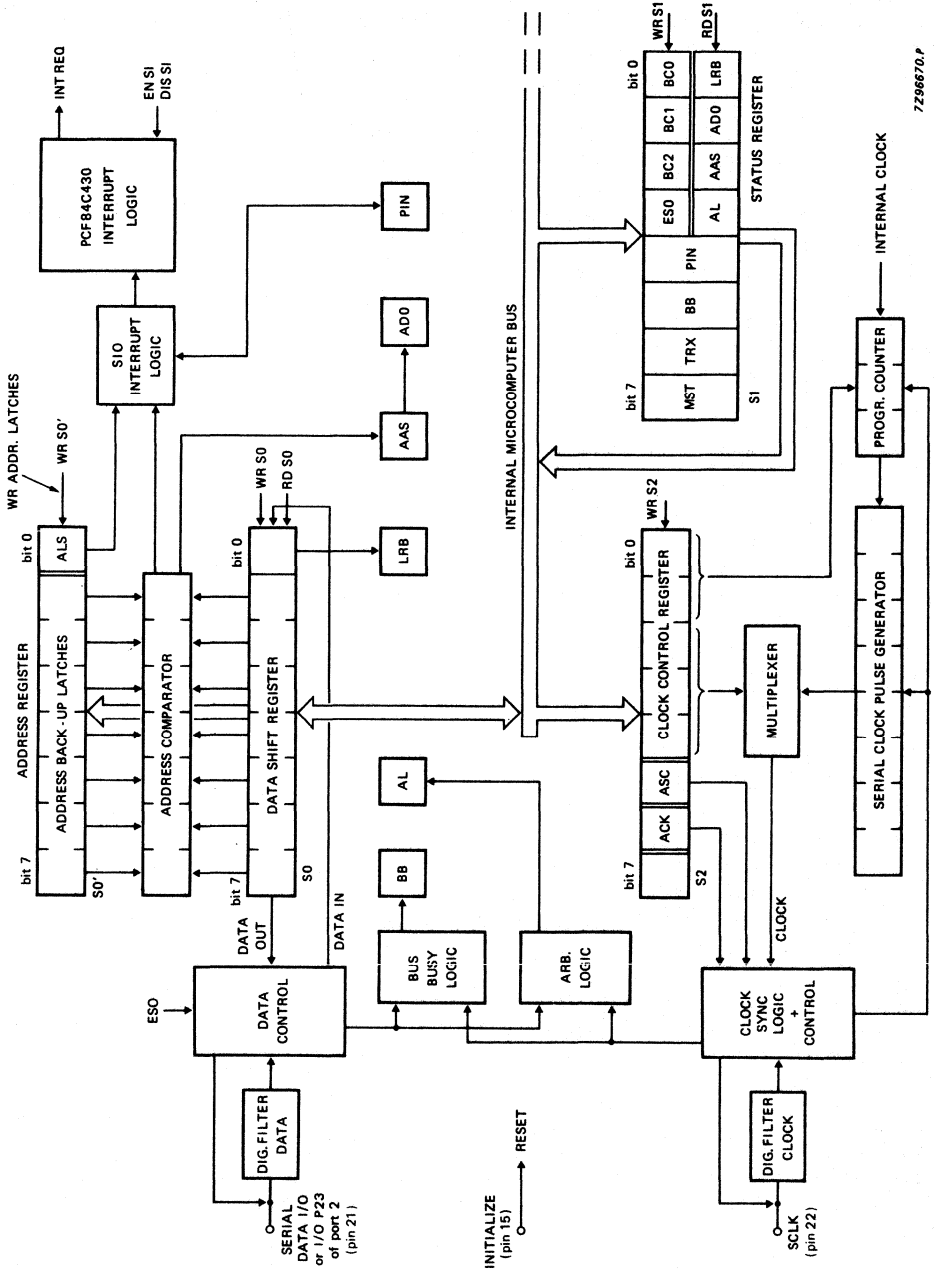


Fig. 13 Serial I/O interface.

Interrupts

Upon entering an interrupt routine, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator must be saved by user software. Interrupt acknowledgement may be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB instructions may not be used within an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, further subroutine calls must be terminated using the RET instruction. Using the RETR instruction to terminate such a nested subroutine would terminate the interrupt routine prematurely.

External interrupt

When the external interrupt is enabled and no interrupt routine is in progress, a HIGH-to-LOW transition on the $\overline{\text{INT}}$/T0 pin sets the External Interrupt Flag (EIF) and invokes the external interrupt routine by forcing a CALL to location 3*. The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency will depend upon the instruction that is being executed when the transition occurs. If an interrupt routine is already in progress, an external interrupt request is stored in the External Interrupt flag (EIF). When the external interrupt is disabled the request is still latched into the digital filter. Execution of a DIS I instruction cancels a stored interrupt request by clearing both the digital filter and the (EIF).

Another external interrupt can be created by enabling the timer/event counter interrupt and loading FFH into the counter (one less than overflow). The STRT CNT instruction is then executed in user software, this enables the event counter mode and a LOW-to-HIGH transition on the T1 input will then initiate an interrupt subroutine and invoke a call to the timer/counter interrupt vector location 7.

SIO Interrupt

An interrupt request from the SIO hardware will set the PIN flag to its active LOW state. This action is fully independant of the Enable SIO interrupt flag. When the SIO interrupt is enabled and no interrupt routine is in progress, the PIN flag at active LOW will invoke the SIO interrupt routine by forcing a CALL to program memory location 5. After the SIO interrupt is initiated, the PIN flag is **not** automatically set back to a HIGH state, this must be done as part of the interrupt subroutine.

Timer/counter Interrupt

When no interrupt routine is in progress and the timer/counter is enabled, a timer/counter overflow sets the Timer interrupt flag (TIF). This initiates the timer interrupt routine by forcing a CALL to program memory location 7**. If an interrupt routine is in progress, the interrupt request is stored in the (TIF) only if the timer interrupt has been enabled. Execution of a DIS TCNTI instruction deletes a previously stored interrupt request. The timer flag (TF) is set every time the timer/counter overflows and is not automatically reset after the timer counter routine is called. It can only be cleared by either the JTF or JNTF or by a hardware RESET.

Interrupt Priority

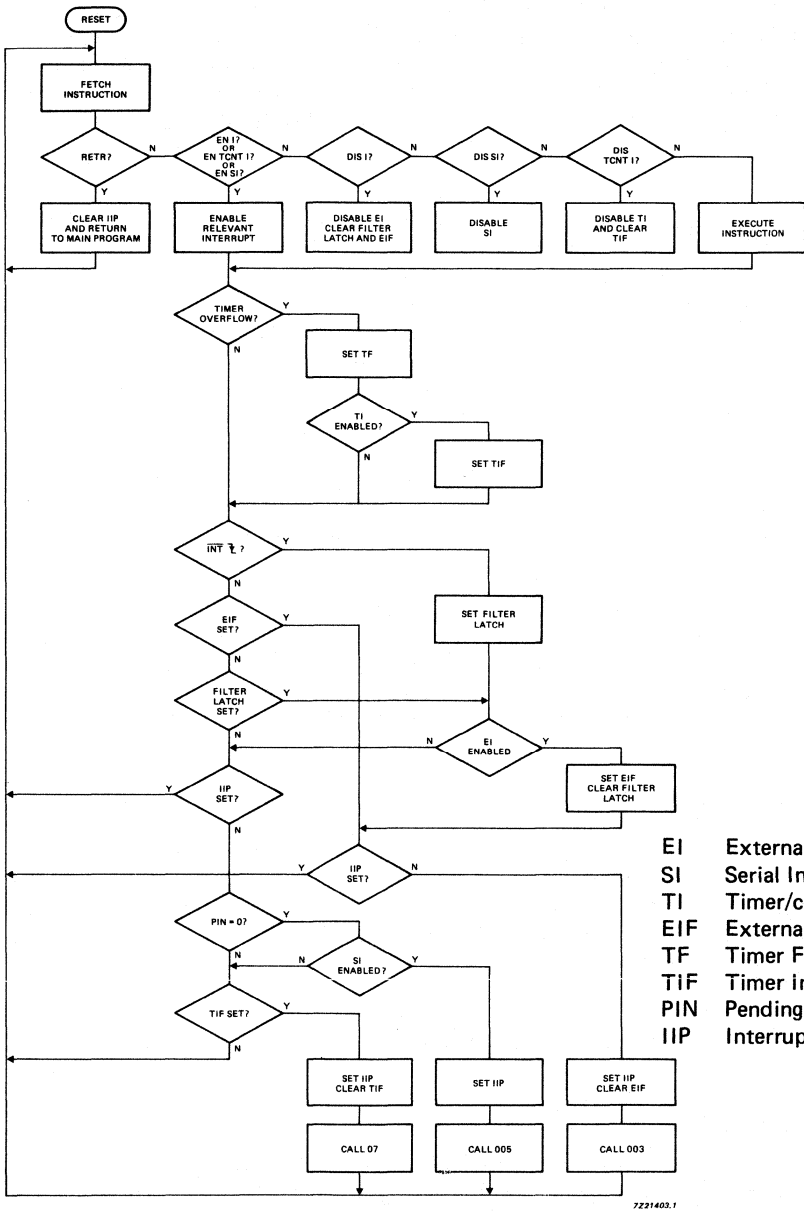
If simultaneous interrupts occur, their priority is as follows:

- External (highest)
- SIO
- Timer/Counter (lowest)

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

* This CALL clears the EIF flag.
** This CALL clears the TIF flag.

FUNCTIONAL DESCRIPTION (continued)



EI	External Interrupt
SI	Serial Interrupt
TI	Timer/counter Interrupt
EIF	External Interrupt Flag
TF	Timer Flag
TIF	Timer Interrupt Flag
PIN	Pending Interrupt NOT (SIO)
IIP	Interrupt In Progress flag

Fig. 14(a) Flow chart illustrating the interrupt handling sequence.

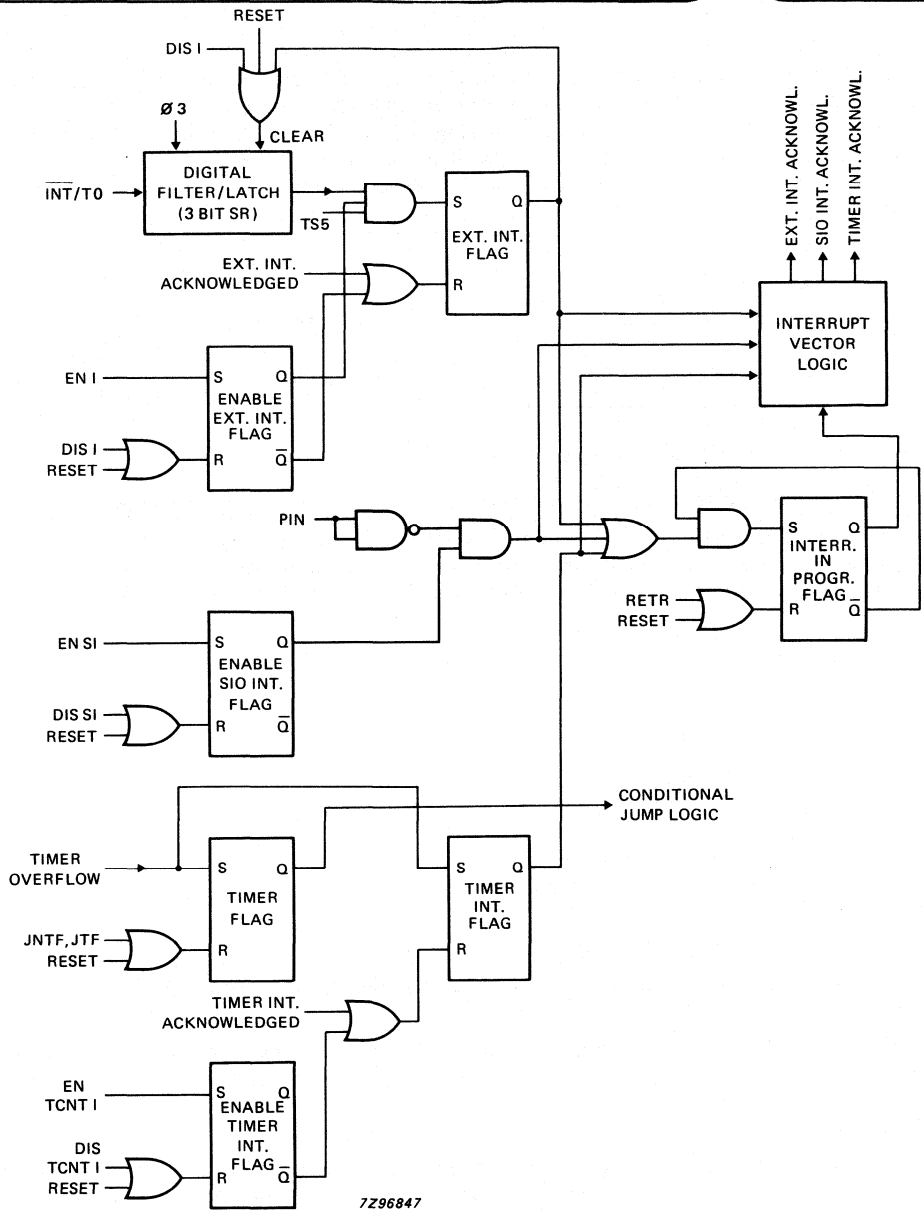


Fig. 14(b) Simplified schematic of interrupt logic, to be used in conjunction with the functional description.

Note to figure

1. $\overline{INT}$/T0 negative edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when $\overline{INT}$/T0 is HIGH for $>$ 4 CP followed by a LOW for $>$ 7 CP.
3. When the interrupt in progress flat is set, further external and timer interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

DEVELOPMENT DATA

Oscillator (see Fig. 15)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range the oscillator will be restarted after a STOP instruction by a LOW level at the $\overline{INT}$/T0 pin or a HIGH level at the RESET pin.

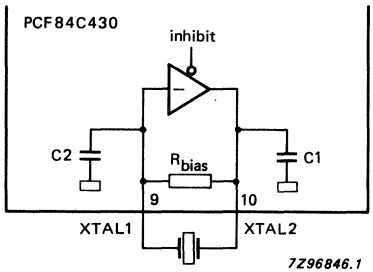


Fig. 15 Oscillator with integrated elements.

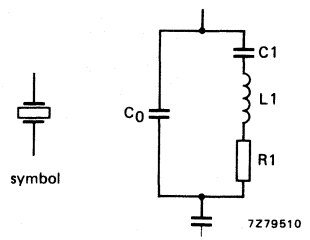


Fig. 16 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_0 + wiring + external capacitors) must not be above the curve (Fig. 17) for the corresponding frequency.
Note: if external capacitors are connected to XTAL 1 and XTAL 2 they must be of equal value.

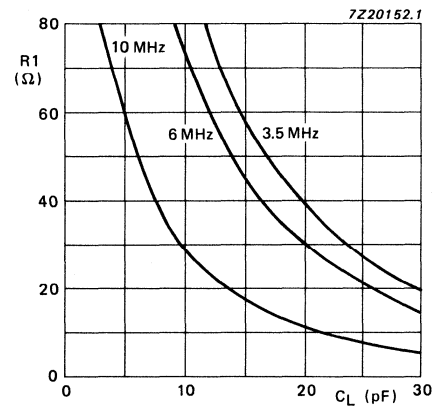


Fig. 17 Crystal circuit series resistance (R1) as a function of load capacitance (C_L).

The oscillator has the output drive capability via pin 10 (XTAL 2). An external clock can be applied to pin 9 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

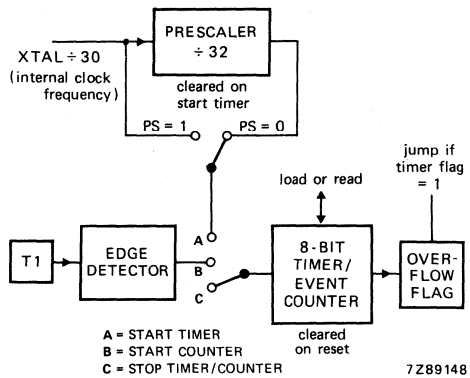
Timer/event counter (see Fig. 18)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin T1 are counted. The counter is incremented during a machine cycle only if the falling edge occurs during the first 7 time slots; otherwise it is incremented during the next cycle. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the Timer flag is set. The flag can be tested and reset using the JTF (jump if Timer flag = logic 1) or JNTF (jump if Timer flag = logic 0) instruction. Overflow also generates an interrupt request to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T



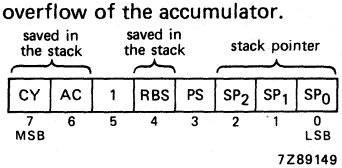
7Z89148 Fig. 18 Timer/event counter.

DEVELOPMENT DATA

Program status word (see Fig. 19)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.



7Z89149 Fig. 19 Program status word.

* With prescaler select, PS = logic 0, the timer is incremented every 32 machine sycles; with PS = logic 1 the timer will be incremented every machine cycle (prescaler not used); the prescaler is cleared by the STRT T instruction and is not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal routine, which is not part of an interrupt subroutine. The RET instruction has no restore feature and must not be used at the end of an interrupt.

Program counter (see Fig. 20)

The 12-bit program counter is able to address 4 K bytes of ROM. The arrangement of the bits is shown in Fig. 20. During an interrupt subroutine PC_{11} is forced to logic 0. All 12 bits are saved in the stack during CALL and interrupt routines.

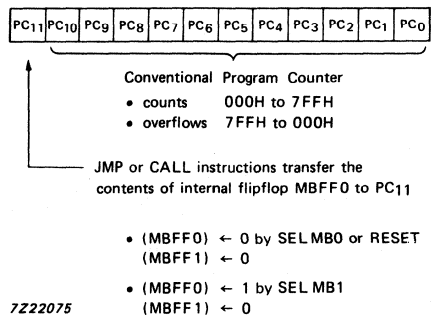


Fig. 20 Program counter.

Central processing unit

The PCF84C430 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JT0
	0	JNT0
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 7)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. A transition can be recognized every 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100$ kΩ). When T1 is not used pin 7 must be connected V_{DD} or V_{SS}.

Reset (pin 15)

A positive-going signal on the RESET input/output

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to divide by 32
- Resets the timer flag
- Sets all ports except P2.3 to input mode (see serial I/O section)
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode
- Re-defines the LCD control byte

A negative-going signal on the RESET input/output:

- Sets P2.3/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the serial I/O to slave receiver mode and disables the serial I/O after a maximum of 30 clock pulses
- Starts program execution after 1866 clock pulses

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Power-on reset

The internal power-on reset circuit monitors the PCF84C430 supply voltage V_{DD}. For as long as the supply voltage remains below the internal reference level V_{ref} (typically 1,5 V) the oscillator is inhibited and RESET (pin 15) has an undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

N.B. Because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three modes of power-on reset are possible:

1. If V_{DD} can be switched with a fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal (t_D) has finished, then no extra components are required (see Fig. 21 and 22). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Fig. 23 and 24). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is >8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant >2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 24). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.
3. Figure 25 shows an external reset to the PCF84C430 during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 26). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

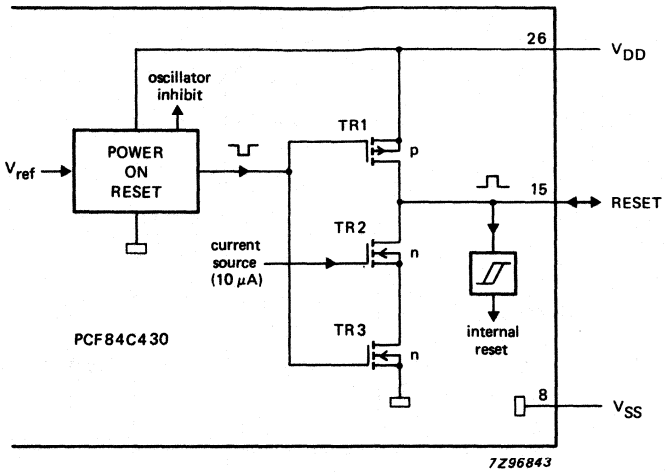


Fig. 21 Power-on-reset configuration.

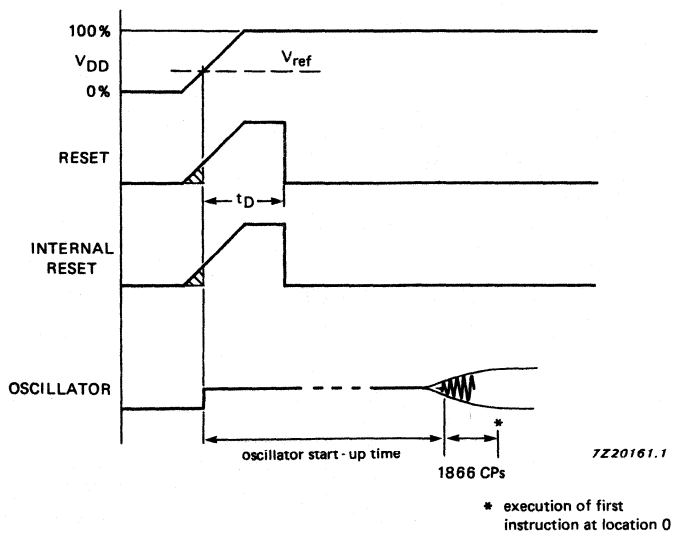


Fig. 22 Timing of power-on-reset with fast rise time.

FUNCTIONAL DESCRIPTION (continued)

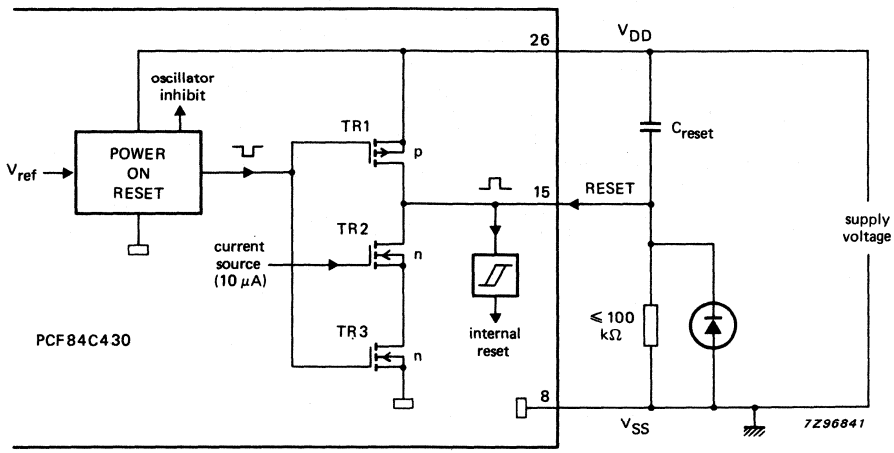


Fig. 23 Stretched power-on-reset with external components.

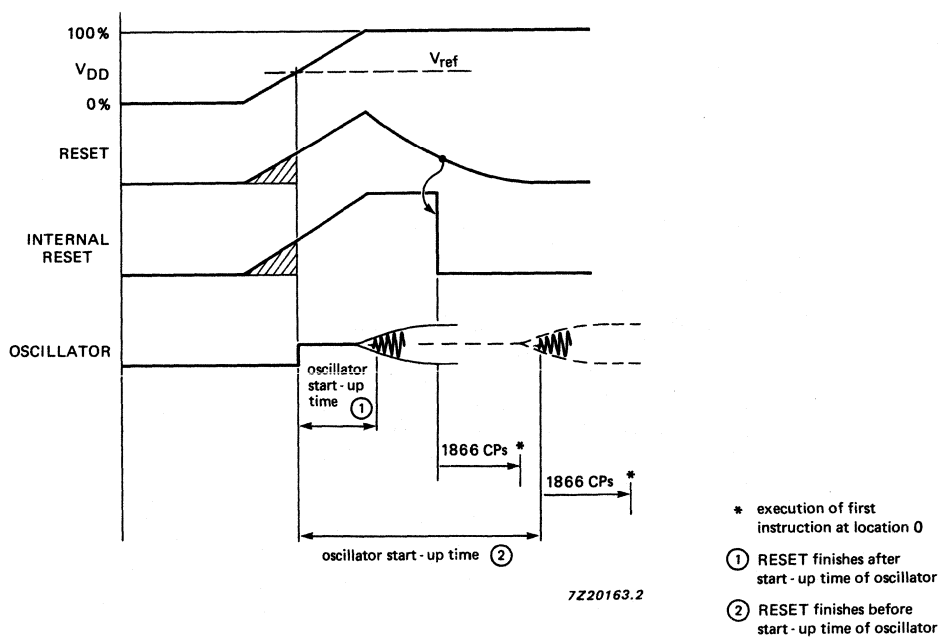


Fig. 24 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

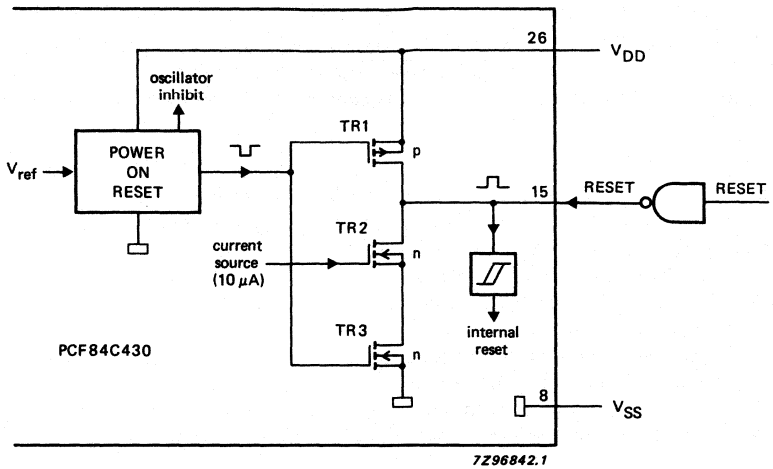


Fig. 25 External power-on-reset configuration.

DEVELOPMENT DATA

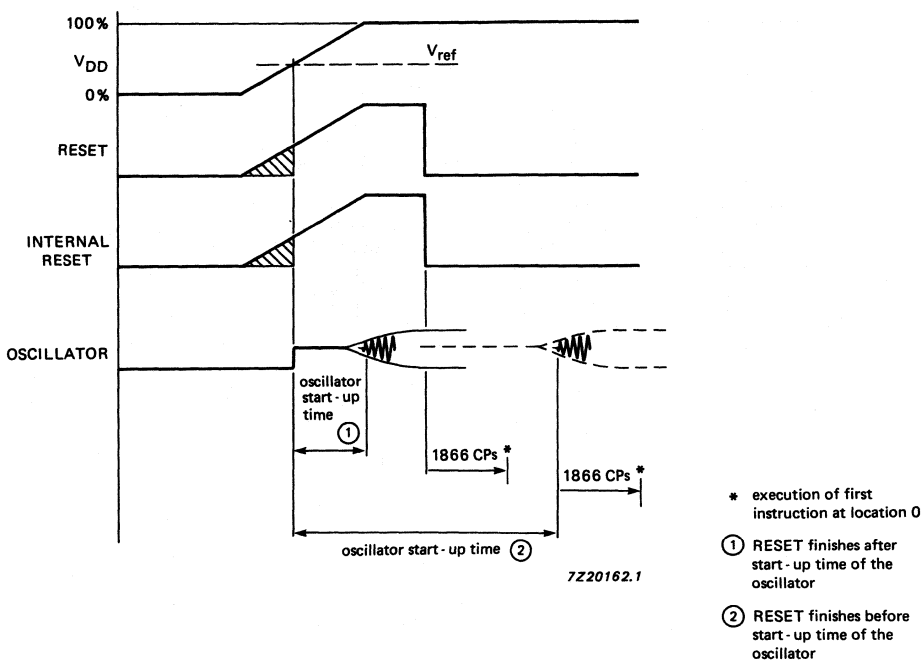


Fig. 26 Timing of external power-on-reset.

FUNCTIONAL DESCRIPTION (continued)

Liquid crystal display driver

The PCF84C430 has a display driver which interfaces to almost any liquid crystal display (LCD) which has a low multiplex rate. The interface delivers drive signals for any static or multiplexed LCD panel that contains up to four backplanes and up to 24 segments. Fig. 27 shows a block diagram of the LCD driver.

The following features are incorporated:

- Selectable backplane drive configuration; static or 2/3/4 backplane multiplexing
- Selectable display bias configuration; 1/2 or 1/3 internal LCD bias generation
- 24 individual segment drivers can be used to provide
  - up to twelve 8-segment numeric characters
  - up to six 15+1 segment alphanumeric characters
  - graphics using up to 96 elements
  - twelve 8-bit derivative registers for display data bits
- LCD and logic voltage supplies may be separated
- An LCD operating voltage range of between V_{SS} to V_{DD} −2,5 V ($V_{SS} \leqslant V_{LCD} \leqslant V_{DD}$)
- A low-power zero-component oscillator keeps the LCD display running in the STOP mode

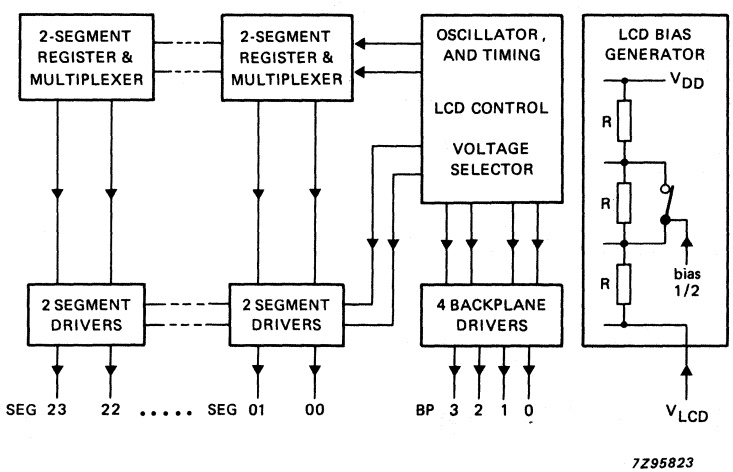


Fig. 27 Block diagram of the LCD driver.

The display configurations possible with the PCF84C430 depend upon the number of active backplane outputs required. A selection of display configurations is given in Table 6.

Table 6 Selection of display configurations

number of backplanes	number of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	5 characters + 2 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 character + 10 indicator symbols	24 dots (1 x 24)

All of the display configurations given in Table 6 can be implemented in the typical system shown in Fig. 28. The appropriate biasing voltages for the multiplexed LCD wave forms are generated internally.

At power-on all the LCD driver control register bits are cleared. The LCD display is not affected by executing a STOP instruction.

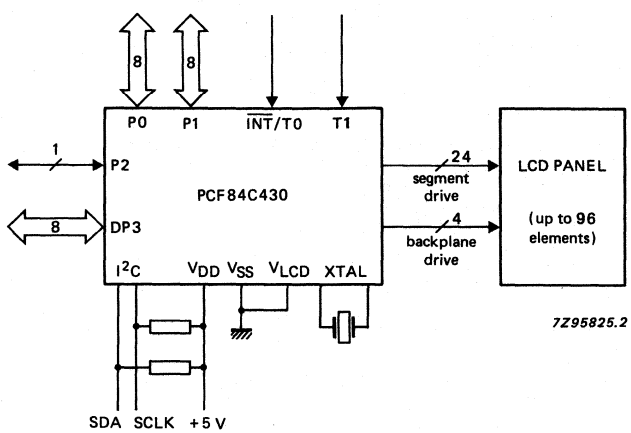


Fig. 28 Typical system configuration.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

LCD bias generation

The LCD operating voltage (V_{op}) is the result of V_{DD} - V_{LCD}. V_{op} should be chosen so that the off voltage ($V_{off(rms)}$) is just below the threshold voltage (V_{th}), typically when the LCD exhibits 10% contrast. The LCD voltage may be temperature compensated externally through the LCD supply. Fractional LCD biasing voltages are obtained from an internal voltage divider of three resistors connected between V_{DD} and V_{LCD}. The centre resistor may be switched out of circuit to provide a ½ bias voltage level for a 1:2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected drive configuration. The operation of the voltage selector is controlled by the MODE bits in the LCD control byte. The biasing configurations that apply to the preferred mode of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and resulting discrimination ratios (D), are given in Table 7.

Table 7 LCD drive modes and characteristics

LCD drive mode	number of backplanes	LCD bias configuration	number of levels	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static	1	static	2	0	1	∞
1:2	2	1/2	3	0,354	0,791	2,236
1:2	2	1/3	4	0,333	0,745	2,236
1:3	3	1/3	4	0,333	0,638	1,915
1:4	4	1/3	4	0,333	0,577	1,7321

Multiplex drive ratios of 1:3 and 1:4 with ½ bias are possible, but the discrimination and contrast ratios are reduced thus;

(1,732 for 1:3 or 1,528 for 1:4)

There is an advantage however, that these modes lead to a reduction in V_{op} as follows:

1:3 multiplex (½ bias). $V_{op} = 2{,}449\ V_{off(rms)}$

1:4 multiplex (½ bias). $V_{op} = 2{,}309\ V_{off(rms)}$

This compares with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD driver (continued)

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms are shown in Fig. 29.

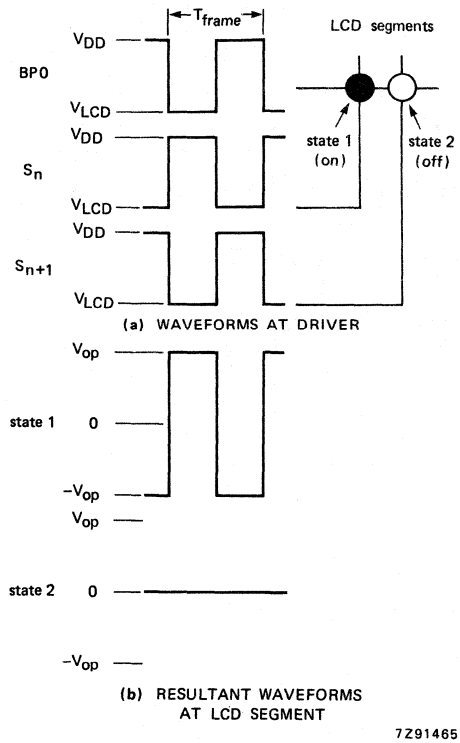


Fig. 29 Static drive mode waveforms.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

When two backplanes are provided in the LCD; the 1:2 multiplex drive mode applies. The PCF84C430 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 30 and 31.

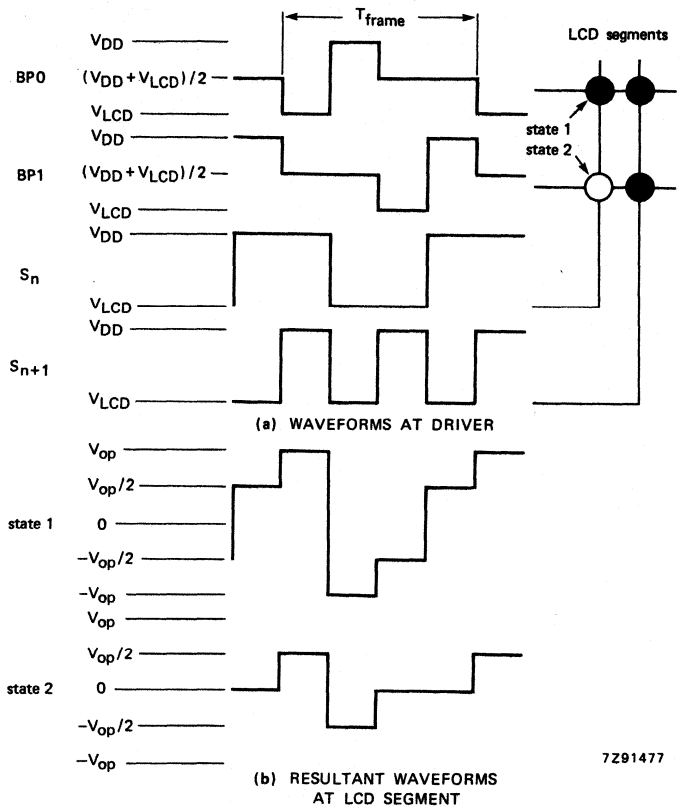


Fig. 30 Waveforms for the 1:2 multiplex drive mode with 1/2 bias.

LCD driver (continued)

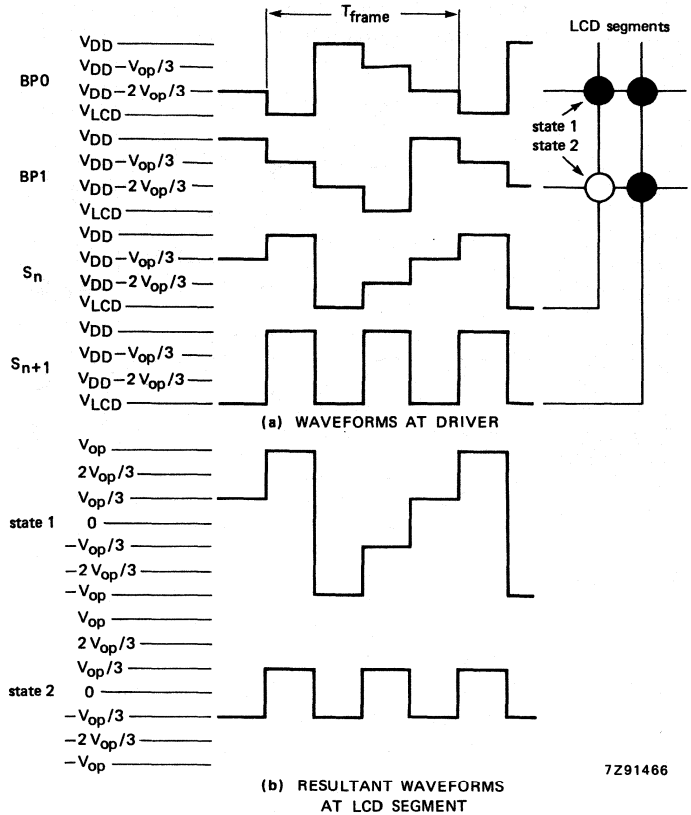


Fig. 31 Waveforms for the 1:2 multiplex drive mode with 1/3 bias.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The backplane and segment drive waveforms for the 1:3 multiplex drive mode (three LCD backplanes) and for the 1:4 multiplex drive mode (four LCD backplanes) are shown in Figs 32 and 33 respectively.

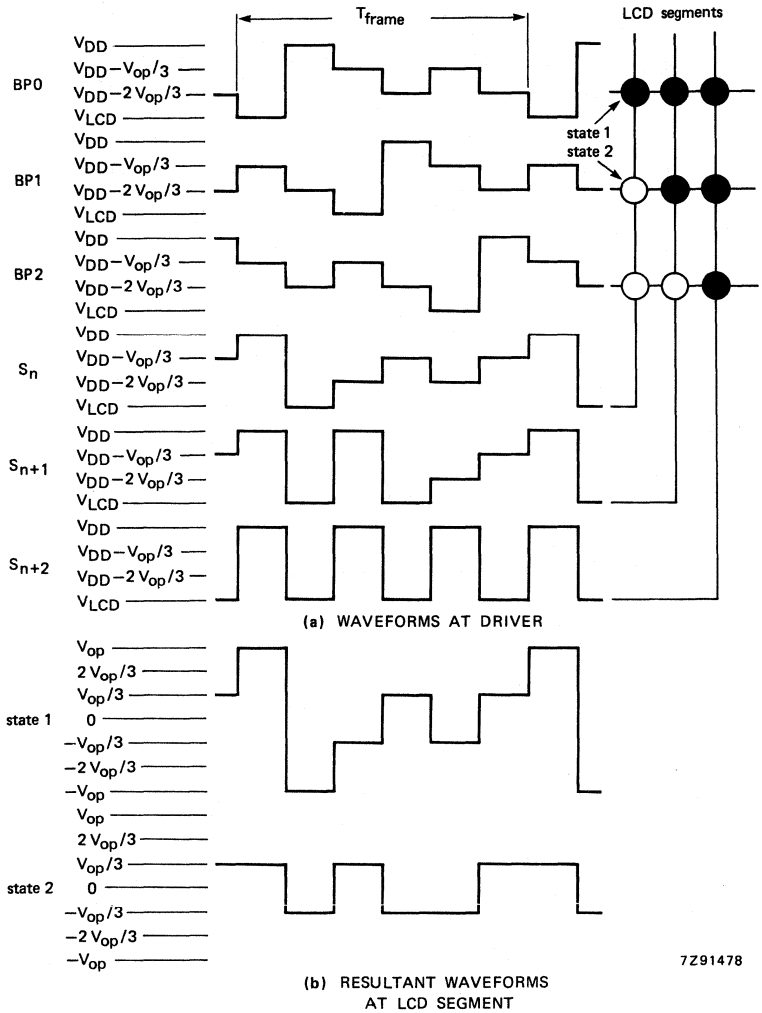


Fig. 32 Waveforms for the 1:3 multiplex drive mode.

LCD driver (continued)

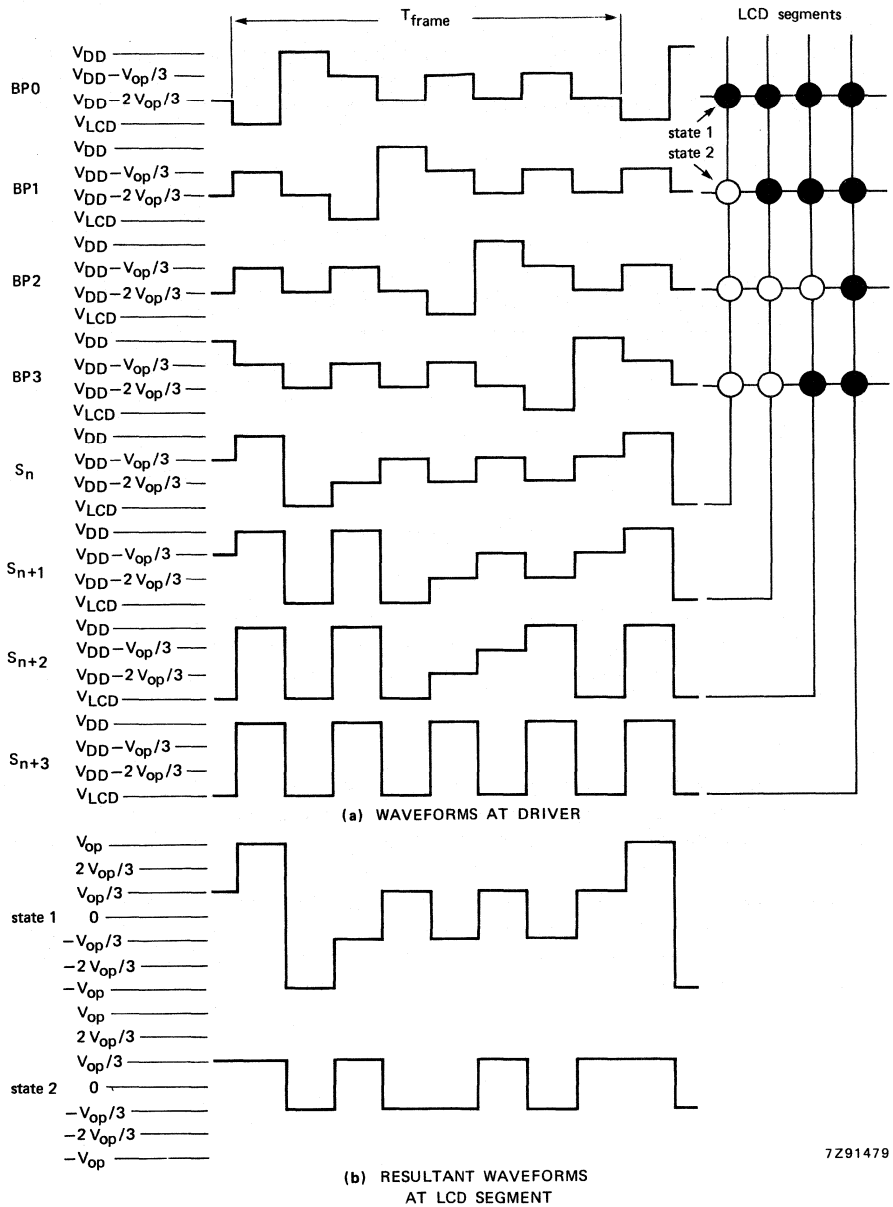


Fig. 33 Waveforms for the 1:4 multiplex drive mode.

FUNCTIONAL DESCRIPTION (continued)

LCD timing

The LCD clocking is performed by a separate, self-contained, on-chip oscillator with a nominal frequency of 30 kHz. The display may be kept active while in the STOP mode using a very low supply current. Fig. 34 shows the LCD timing control.

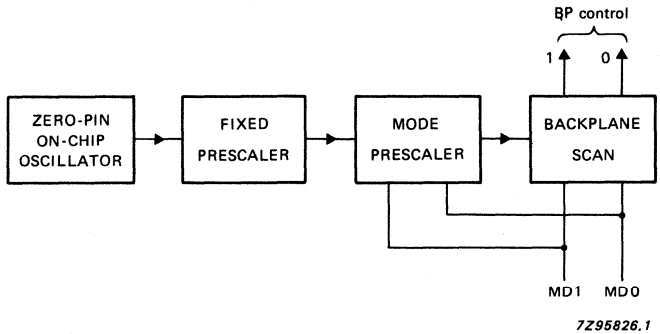


Fig. 34 LCD timing control.

LCD segment driver outputs

The LCD drive section includes 24 segment outputs (S0 to S23) which should be connected directly to the LCD. The segment data bits (one nibble per segment) are multiplexed to the outputs in accordance with the backplane signals. If less than the 24 segment outputs are required then the unused driver outputs should be left open.

Backplane outputs

The LCD drive section includes 4 backplane outputs (BP0-BP3) which should be connected directly to the LCD. These backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required then the unused driver outputs should be left open-circuit.

In the 1:3 multiplex drive mode, BP3 carries the same signal as BP0, therefore these two outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP3, BP1 and BP2 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and may be connected in parallel to give a very high drive capability.

LCD driver (continued)

LCD segment display registers

The 12 segment display registers are 8-bit derivative (read/write) registers which store LCD segment data. A segment register bit which is set to a logic 1 indicates the 'on' state of the corresponding LCD segment, similarly, a logic 0 indicates the 'off' state. There is a one-to-one relationship between the LCD segment register bits and the segment outputs. Every byte is divided into two nibbles. Each nibble corresponds to a segment driver; the first byte contains the bits earmarked for segment 1 and 2 etc. The first bit of a nibble will correspond to backplane 0, and the second to backplane 1 and so on. Fig. 35 shows the display register bit map. Each bit is shown in the form Sxx.n, where (xx) is the segment output and (n) the backplane output.

LCDD : LCD display data

17	R/W	S 0.0	S 0.1	S 0.2	S 0.3	S 1.0	S 1.1	S 1.2	S 1.3
18	R/W	S 2.0	S 2.1	S 2.2	S 2.3	S 3.0	S 3.1	S 3.2	S 3.3
19	R/W	S 4.0	S 4.1	S 4.2	S 4.3	S 5.0	S 5.1	S 5.2	S 5.3
20	R/W	S 6.0	S 6.1	S 6.2	S 6.3	S 7.0	S 7.1	S 7.2	S 7.3
21	R/W	S 8.0	S 8.1	S 8.2	S 8.3	S 9.0	S 9.1	S 9.2	S 9.3
22	R/W	S10.0	S10.1	S10.2	S10.3	S11.0	S11.1	S11.2	S11.3
23	R/W	S12.0	S12.1	S12.2	S12.3	S13.0	S13.1	S13.2	S13.3
24	R/W	S14.0	S14.1	S14.2	S14.3	S15.0	S15.1	S15.2	S15.3
25	R/W	S16.0	S16.1	S16.2	S16.3	S17.0	S17.1	S17.2	S17.3
26	R/W	S18.0	S18.1	S18.2	S18.3	S19.0	S19.1	S19.2	S19.3
27	R/W	S20.0	S20.1	S20.2	S20.3	S21.0	S21.1	S21.2	S21.3
28	R/W	S22.0	S22.1	S22.2	S22.3	S23.0	S23.1	S23.2	S23.3

Fig. 35 Display register bit map.

In the static drive mode the eight display data bits are placed in bit 0 of the nibbles of four successive derivative display registers. In the 1:2 multiplex drive mode, these eight bits are placed in bits 0 and 1 of the nibbles of two successive registers. In the 1:3 multplex drive mode the eight bits are placed in

FUNCTIONAL DESCRIPTION (continued)

bits 0, 1 and 2 of three successive nibbles. In the 1:4 multiplex drive mode the eight bits are placed in bits 0, 1, 2 and 3 of the nibbles of the first display register. Fig. 36 shows the relationship between LCD segment layout, drive mode and the LCD segment derivative register bit pattern.

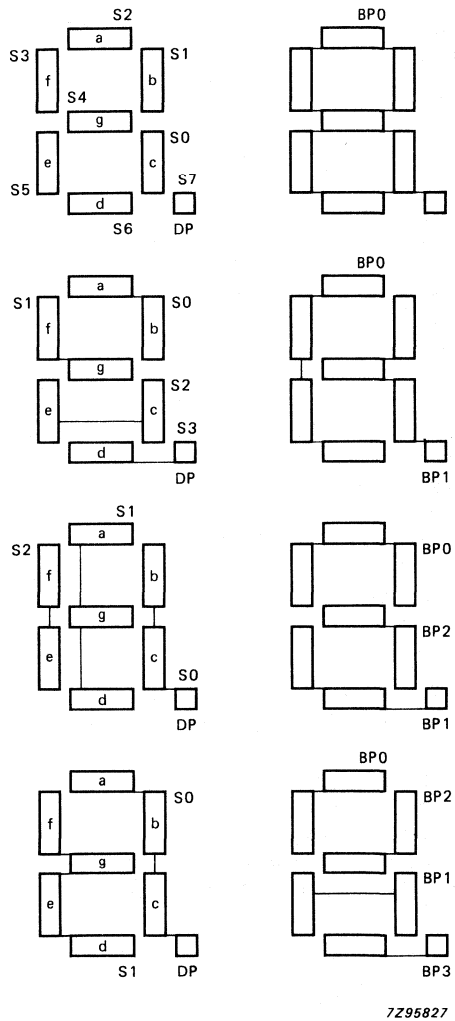


Fig. 36 LCD segment layout and register bit pattern.

LCD derivative register bit map

byte

17	c	–	–	–	b	–	–	–
18	a	–	–	–	f	–	–	–
19	g	–	–	–	e	–	–	–
20	d	–	–	–	Dp	–	–	–

static mode

byte

17	a	b	–	–	f	g	–	–
18	e	c	–	–	d	Dp	–	–
19	–	–	–	–	–	–	–	–
20	–	–	–	–	–	–	–	–

1:2 multiplex mode

byte

17	b	Dp	c	–	a	d	g	–
18	f	e	–	–	–	–	–	–
19	–	–	–	–	–	–	–	–
20	–	–	–	–	–	–	–	–

1:3 multiplex mode

byte

17	a	c	b	Dp	f	e	g	d
18	–	–	–	–	–	–	–	–
19	–	–	–	–	–	–	–	–
20	–	–	–	–	–	–	–	–

1:4 multiplex mode

LCD driver (continued)

LCD control register

The LCD operating mode is governed by four bits of the LCD control register (address 16 D). The LCD control register is an 8-bit derivative read/write register. The function of each bit is given in Table 8.

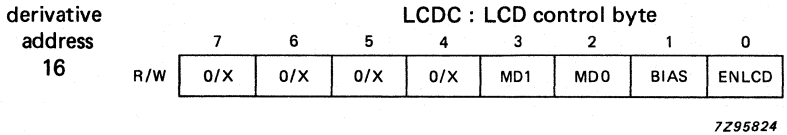


Table 8 Control register bit definition

bit	name	function		
0	ENLCD	0 = LCD display disabled 1 = LCD display enabled		
1	BIAS	0 = 1/3 V_{DD} 1 = 1/2 V_{DD}		
2, 3	MD0/MD1	MD1	MD0	multiplex mode
		0 0 1 1	0 1 0 1	static 1:2 1:3 1:4
4-7	unused			

ENLCD: When ENLCD is reset to 0, the LCD is disabled. Consequently all segment and backplane drivers are set to the V_{DD} level. When ENLCD is set to a 1, the LCD is enabled and character display is possible.

BIAS: The BIAS bit sets the LCD voltage bias generator to either 1/2 or 1/3 of V_{DD}, see Fig. 27.

MD0/MD1: Mode bits MD0 and MD1 determine the multiplex rate. Four multiplex rates are available; static, 1:2, 1:3 and 1:4.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

LCD control byte after RESET

After an external or power-on reset the LCD control register is set with 0C H.

	7	6	5	4	3	2	1	0
	0/X	0/X	0/X	0/X	MD1	MD0	BIAS	ENLCD
reset value	0	0	0	0	1	1	0	0

7Z97990

- The LCD is disabled and segment and backplane drives are switched to the V_{DD} level.
- BIAS is set to generate 1/3 V_{DD}.
- Bits MD0 and MD1 reset the multiplex mode to the 1:4 mode.

INSTRUCTION SET

The PCF84C430 instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 11 gives the instruction set of the PCF84C430. Table 10 shows the instruction map and Table 9 details the symbols and definition descriptions that are used.

Table 9 Symbols and definitions used in Table 11

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	Derivative register designation (x = 4,5,16,17-28)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

INSTRUCTION SET (continued)

Table 10 PCF84C430 instruction map

first hexadecimal character of opcode ↓ \ second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp				MOV A,Sn			
									0	1	2		0	1		
1	INC @Rr		JBO addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
	0	1							0	1	2	3	4	5	6	7
2	XCH A,@Rr		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr							
	0	1							0	1	2	3	4	5	6	7
3	XCHD A,@Rr		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A				MOV Sn,A			
	0	1							0	1	2		0	1	2	
4	ORL A,@Rr		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
	0	1							0	1	2	3	4	5	6	7
5	ANL A,@Rr		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
	0	1							0	1	2	3	4	5	6	7
6	ADD A,@Rr		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
	0	1							0	1	2	3	4	5	6	7
7	ADDC A,@Rr		JB3 addr		CALL page 3			RR A	ADDC A,Rr							
	0	1							0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data				MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
									0	1	2					
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data				MOV Sn,#data			
									0	1	2		0	1	2	
A	MOV @Rr,A			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A							
	0	1							0	1	2	3	4	5	6	7
B	MOV @Rr,#data		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data							
	0	1							0	1	2	3	4	5	6	7
C	DEC @Rr				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr							
	0	1							0	1	2	3	4	5	6	7
D	XRL A,@Rr		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr							
	0	1							0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr							
	0	1							0	1	2	3	4	5	6	7
F	MOV A,@Rr		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr							
	0	1							0	1	2	3	4	5	6	7

Table 11 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

INSTRUCTION SET (continued)

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1	r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1		
BRANCH	JMP addr	● 4 addr	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
	DJNZ Rr, addr	E* addr	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
	DJNZ @Rr, addr	E0 addr	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr		
		E1 addr			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr		
	JBb addr	▲ 2 addr	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr	b = 0–7	
	JC addr	F6 addr	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr		
	JNC addr	E6 addr	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr		
	JZ addr	C6 addr	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr		
	JNZ addr	96 addr	2/2	jump to addr if A is NOT zero	if A ≠ 0 : (PC_{0-7})←addr		
	JT0 addr	36 addr	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
	JNT0 addr	26 addr	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
	JT1 addr	56 addr	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
	JNT1 addr	46 addr	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
	JTF addr	16 addr	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4
	JNTF addr	06 addr	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr		

INSTRUCTION SET (continued)

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	10
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	10
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 addr	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4,6,7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4,6,7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C direct	2/2	Move derivative register/port contents addressed by direct to accumulator	(A)←(Dx) x = 4,5,16,17-28	8
	MOV Dx, A	8D direct	2/2	Move contents of accumulator to derivative register addressed by direct	(Dx)←(A) x = 4,16,17-28	8
	ANL Dx, A	8E direct	2/2	AND contents of accumulator with derivative register addressed by direct	(Dx)←(Dx) AND (A) x = 4,16,17-28	8
	ORL Dx, A	8F direct	2/2	OR contents of accumulator with derivative register addressed by direct	(Dx)←(Dx) OR (A) x = 4,16,17-28	8

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8,9,A,B,C,D,E,F
● : 0,2,4,6,8,A,C,E
▲ : 0,3,5,7,9,B,D,F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000 (P23) 111
8. Dx = 04, 05, 16, 17-28
9. (S1) has a different function in read and write operations, see serial I/O interface.
10. SEL MB0 and SEL MB1 must not be used within interrupt routines.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 26)	V_{DD}	−8	+ 8	V
All input voltages	V_I	−0,8	V_{DD} + 0,8	V
DC current into input or output	$\pm I_I \pm I_O$	−	10	mA
Power dissipation per output				
(not P2.3 and SCLK)	P_O	−	50	mW
(P2.3 and SCLK only)	P_O	−	180	mW
Storage temperature	T_{stg}	−65	+ 150	°C
Ambient operating temperature range (if P_{tot}max. = 100 mW)	T_{amb}	−40	+ 70	°C
Ambient operating temperature range (if P_{tot}max. = 30 mW)	T_{amb}	−40	+ 85	°C
Operating junction temperature	T_j	−	90	°C

DEVELOPMENT DATA

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

LCD DRIVER CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C. All voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
LCD supply voltage (note 1)	V_{LCD}	V_{SS}	−	$V_{DD}-2,5$	V
DC voltage component (BP0 to BP3) at C_{BP} = 35 nF	$+/-V_{BP}$	0	20	−	mV
DC voltage component (S0 to S23) at C_S = 5 nF	$+/-V_S$	−	20	−	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{SS}$ (note 2)	R_{BP}	−	−	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{SS}$ (note 2)	R_S	−	−	7,0	kΩ
Driver delays with test loads at $V_{LCD} = V_{SS}$	tp_{LCD}	−	−	1,0	μs
LCD scan frame frequency	f_{LCD}	−	65	−	Hz

Notes to the LCD driver characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs measured one at a time.

DC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

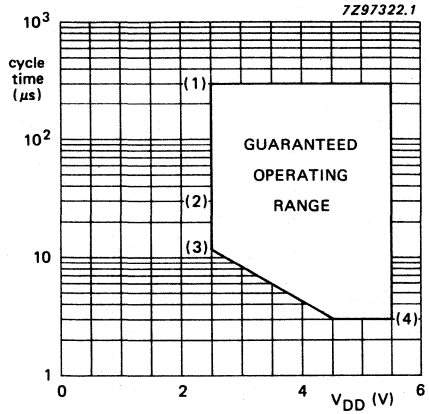
parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 37)	V_{DD}	2,5	–	5,5	V
Supply current					
operating (see Fig. 38)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1,6	3,2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,3	0,6	mA
IDLE mode (see Figs 39 and 40)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	0,5	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,15	0,4	mA
STOP mode (see Fig. 45 and note 1)					
at V_{DD} = 2,5 V; T_{amb} = 25 °C	I_{DD}	–	1,2	*	μA
at V_{DD} = 2,5 V; T_{amb} = 85 °C	I_{DD}	–	–	*	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P2.3/SDA, SCLK (see Fig. 42)	I_{OL}	1,6	3	–	mA
P2.3/SDA, SCLK (see Fig. 42)	I_{OL}	3	–	–	mA
Pull-up output source current HIGH (see Fig. 43)					
at V_{DD} = 5 V ± 10%; $V_O = 0{,}7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; $V_O = V_{SS}$	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; $V_O = V_{DD}-0{,}4$ V	$-I_{OH}$	1,6	3	–	mA

Note to the DC characteristics

1. Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via a 5,6 kΩ resistor; T1 at V_{SS}, $\overline{INT}$ at V_{DD}.

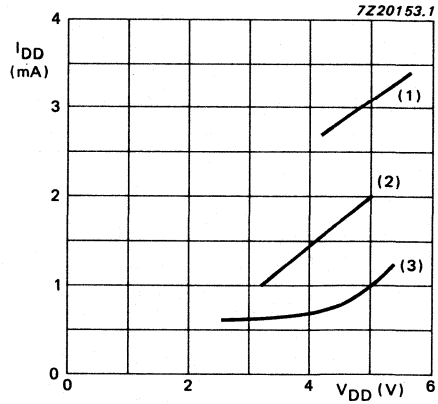
* Value to be fixed.

AC CHARACTERISTICS



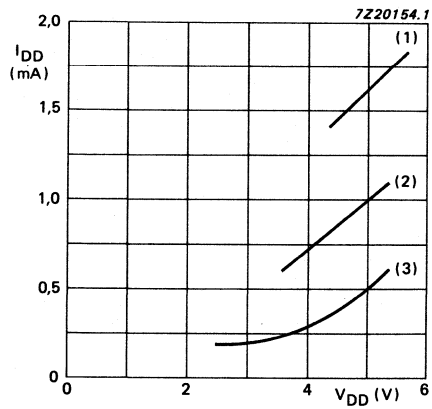
(1) clock frequency = 100 kHz
(2) clock frequency = 1 MHz
(3) clock frequency = 3 MHz
(4) clock frequency = 10 MHz

Fig. 37 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 38 Maximum supply current (I_{DD}) in operating mode as a function of the supply voltage.



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 39 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).

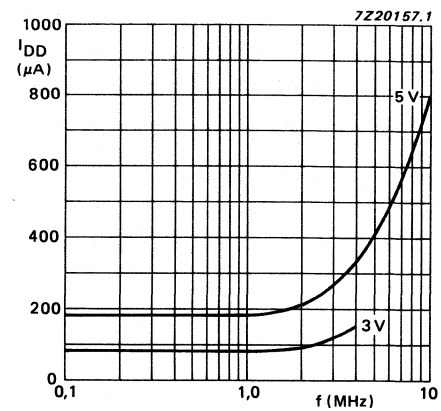


Fig. 40 Typical supply current during IDLE mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

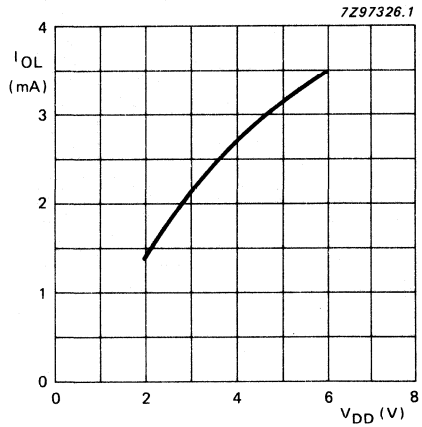


Fig. 41 Typical output sink current (I_{OL}), outputs P0.0 to P0.7 and P2.0 to P2.2, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

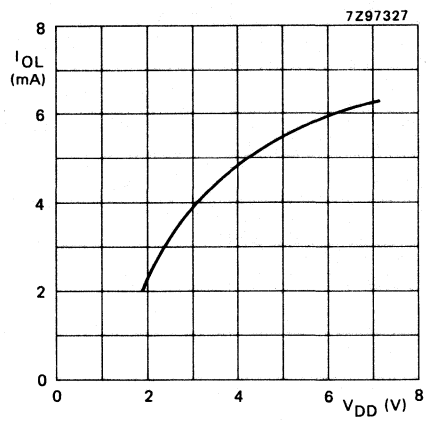


Fig. 42(a) Typical output sink current (I_{OL}), outputs P2.3/SDA and SCLK, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

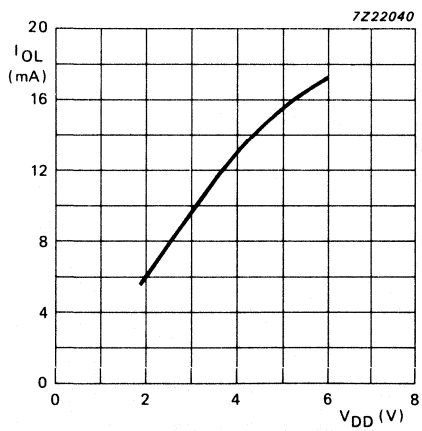
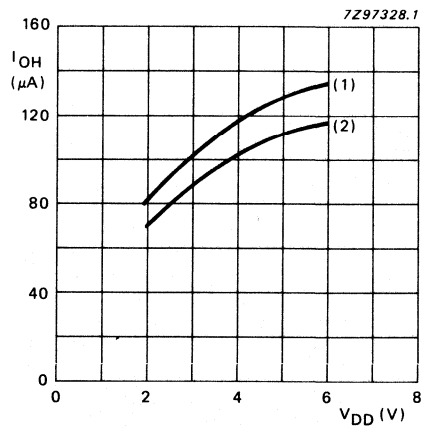


Fig. 42(b) Typical output sink current (I_{OL}), outputs P1.0 to P1.7, as a function of the supply voltage (V_{DD}); V_O = 1,2 V.



(1) $V_O = V_{SS}$
(2) $V_O = 0{,}7\ V_{DD}$
Fig. 43 Typical output source current ($-I_{OH}$) as a function of the supply voltage (V_{DD}).

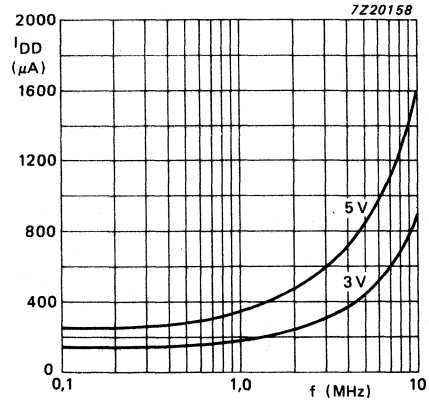
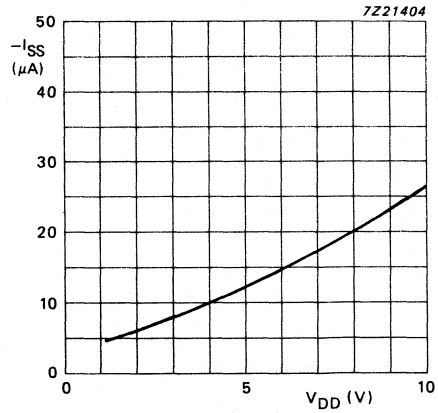


Fig. 44 Typical supply current during operating mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.



$f_{CLK} \triangleq 30$ kHz
$T_{amb} = 85$ °C

Fig. 45 Typical supply current ($-I_{SS}$) in STOP mode as a function of the supply voltage (V_{DD}).

DEVELOPMENT DATA

Table 12 Input timing shown in Fig. 46

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1$ μs
t_{RC}	$\leqslant 1$ μs
t_{FD}	$\leqslant 1$ μs
t_{FC}	$\leqslant 0{,}3$ μs

Notes to Table 12

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
These figures apply to all modes.

AC CHARACTERISTICS (continued)

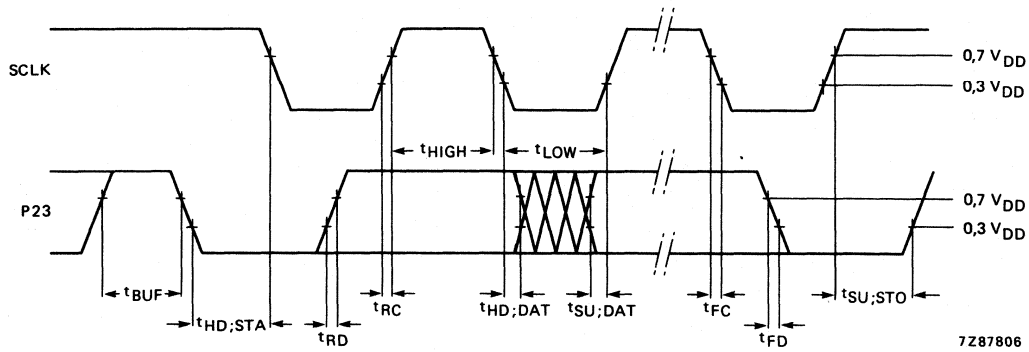


Fig. 46 PCF84C430 timing requirements for the P2.3 and SCLK *input* signals.

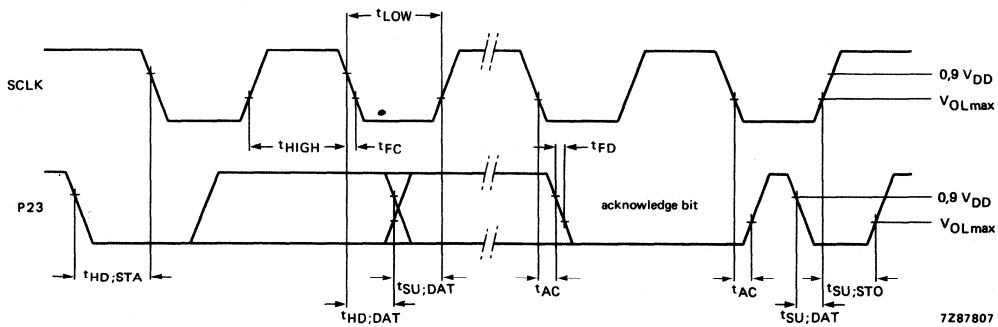


Fig. 47 PCF84C430 timing requirements for the P2.3 and SCLK *output* signals.

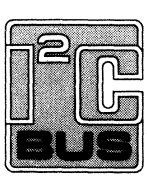
Table 13 Output timing shown in Fig. 47

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1
$t_{HD;STA}$	$\frac{1}{2}$ (DF + 9) t_{XTAL}	$\frac{3}{4}$ (DF + 9) t_{XTAL}
t_{HIGH}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{3}{4}$ (DF) t_{XTAL}
t_{LOW}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{1}{4}$ (DF) t_{XTAL}
$t_{SU;STO}$	$\frac{1}{2}$ (DF − 3) t_{XTAL}	$\frac{1}{4}$ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	– –	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{FD};t_{FC}$	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 13

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
DF = divisor (see Table 3 Serial I/O section).
C_b = the maximum bus capacitance for each line.

DEVELOPMENT DATA



REMOTE 8-BIT I/O FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C bus
- Peripheral for the MAB8400 and PCF8500 microcomputer families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)

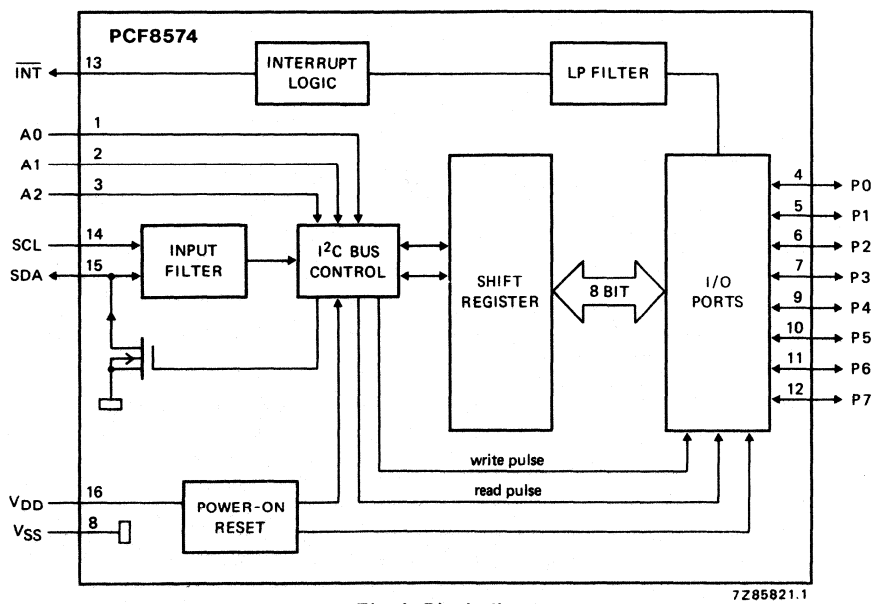


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P: 16-lead DIL; plastic (SOT-38).
PCF8574T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

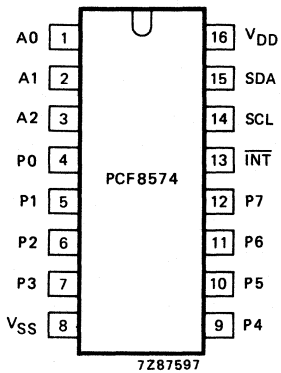


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

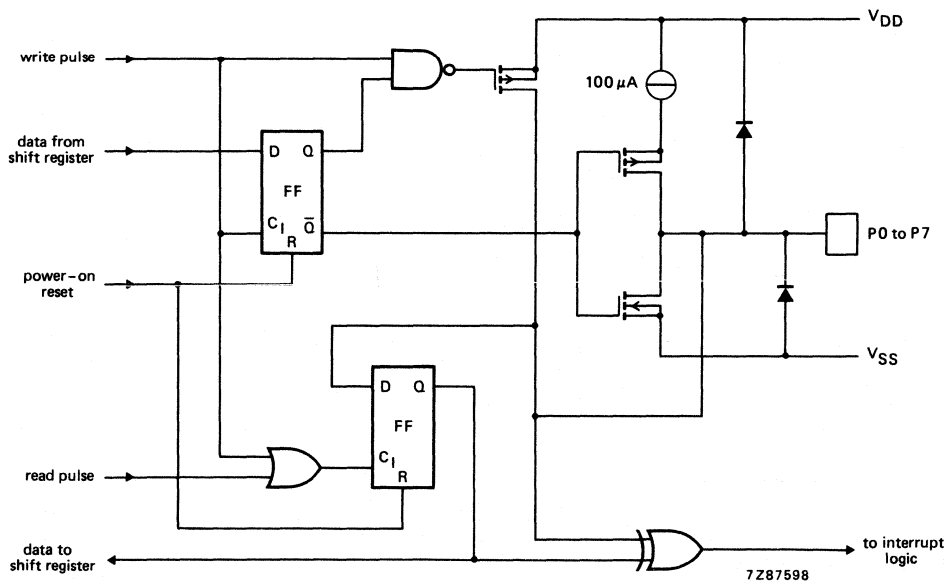


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

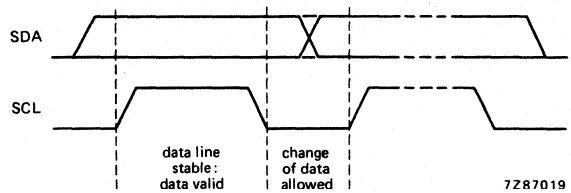


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

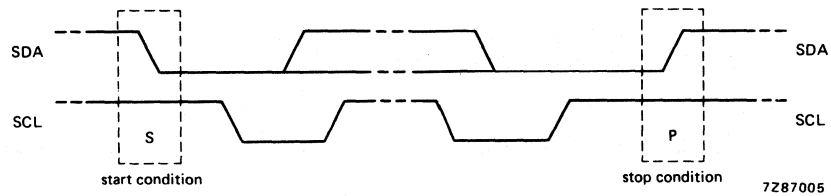


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

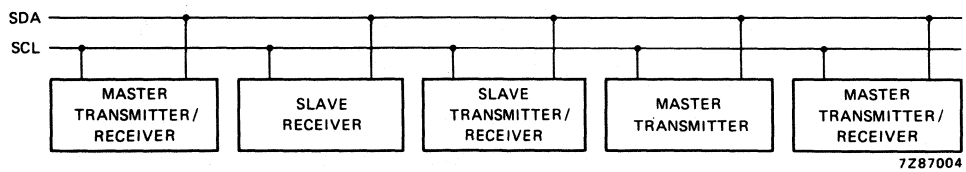


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

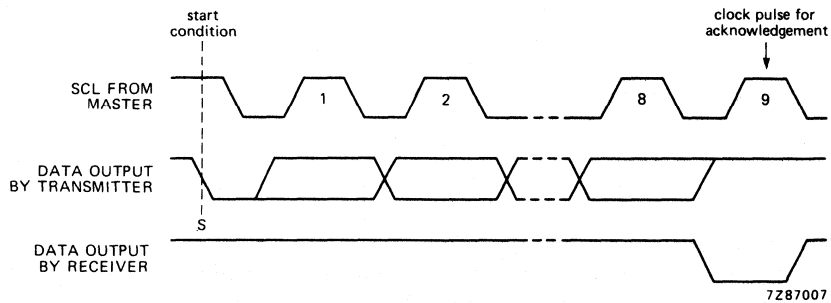


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

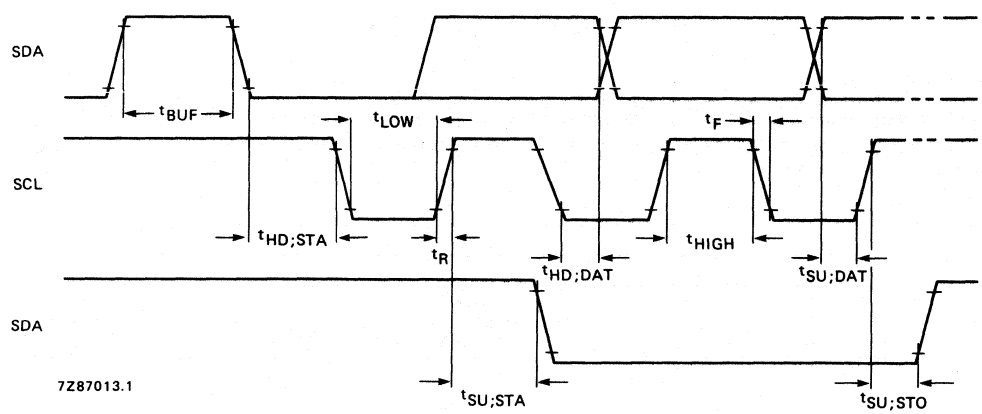


Fig. 8 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

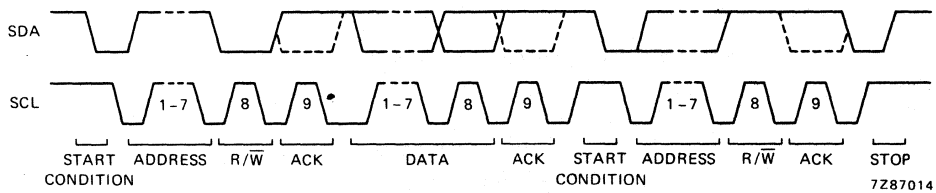


Fig. 9 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 10.

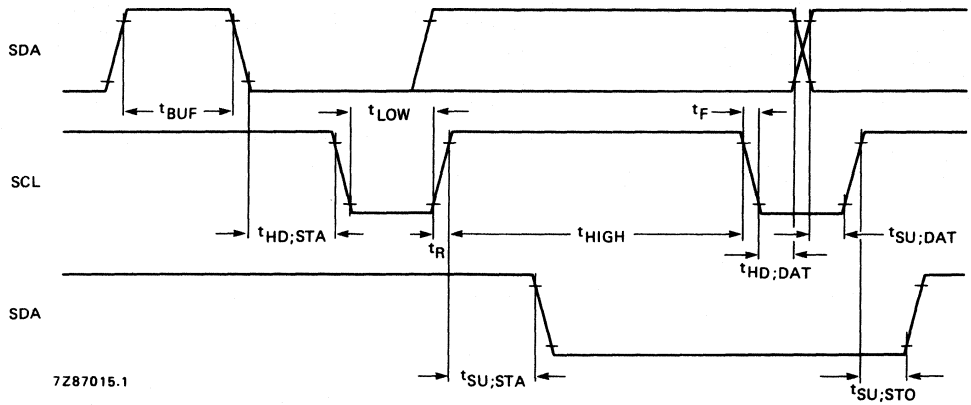


Fig. 10 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

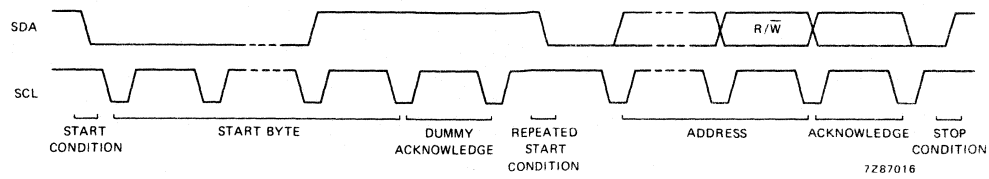


Fig. 11 Complete data transfer in the low-speed mode.

Where:	
Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 12 and 13)

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

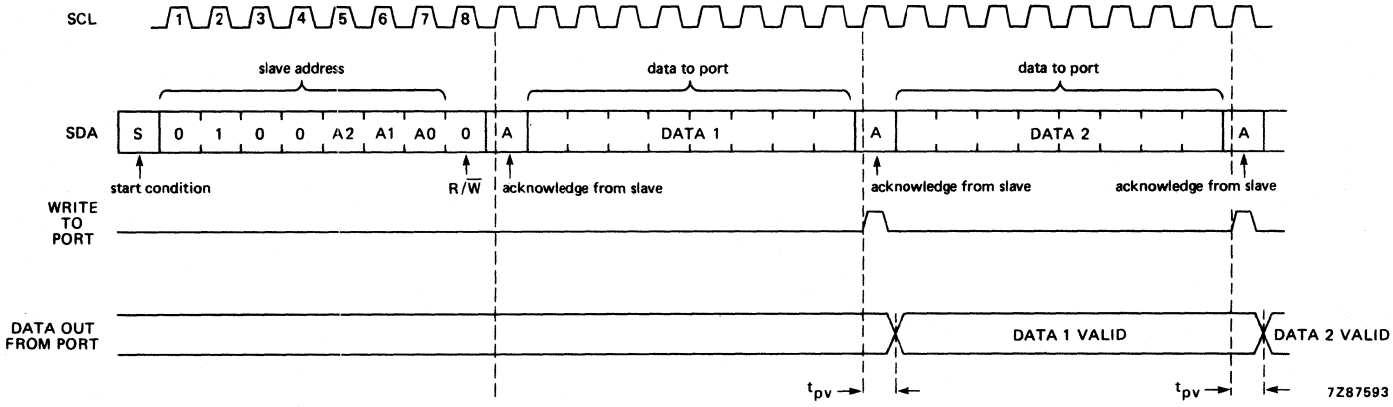


Fig. 12 WRITE mode (output port).

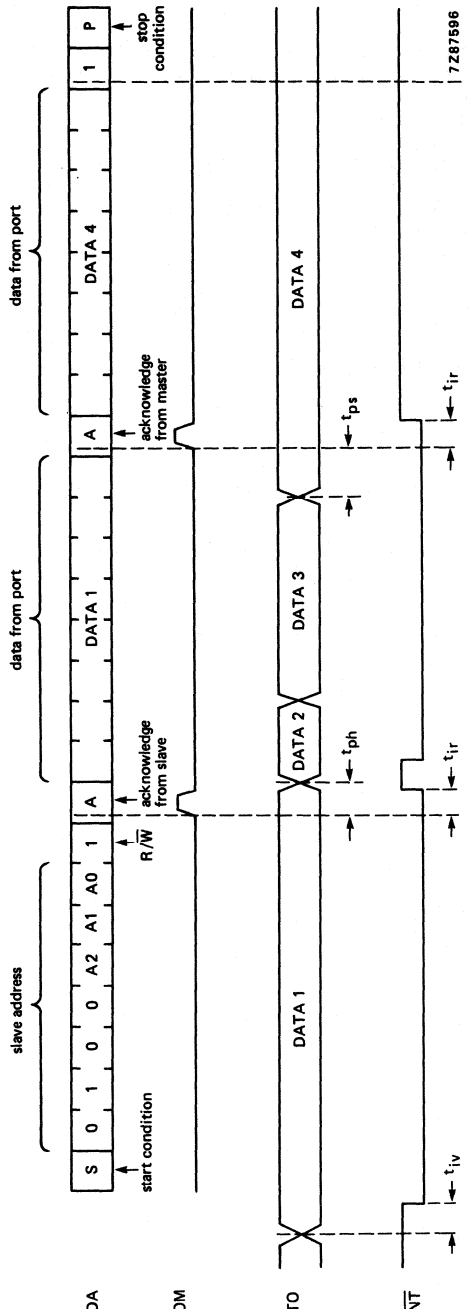


Fig. 13 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 14 and 15)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

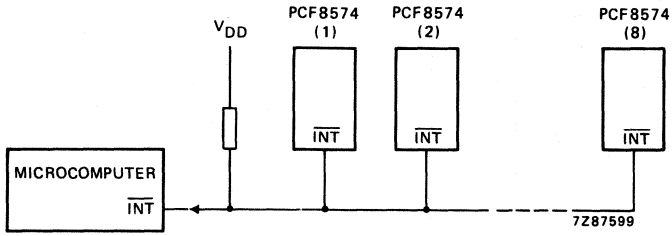


Fig. 14 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

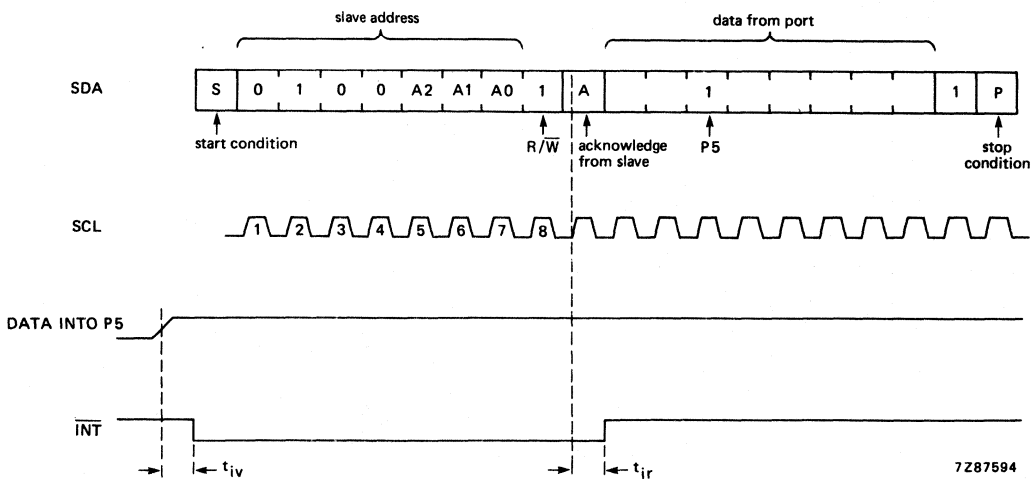


Fig. 15 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 16)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

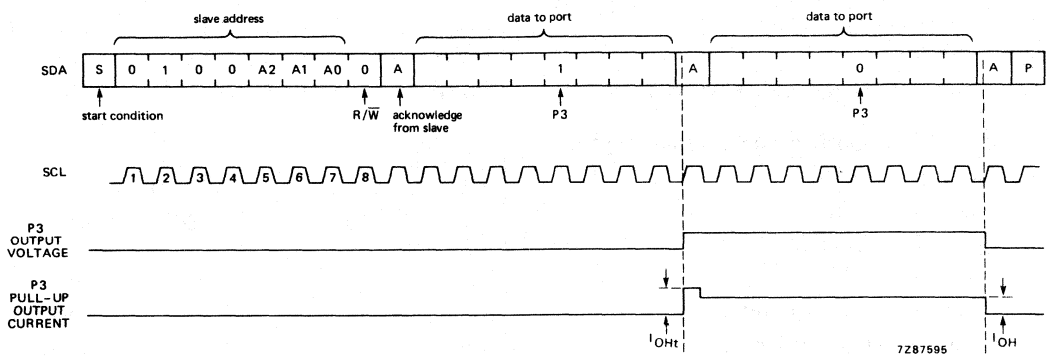


Fig. 16 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7	V
Input voltage range (any pin)	V_I		V_{SS}−0,5 to V_{DD} + 0,5	V
D.C. current into any input	$\pm I_I$	max.	20	mA
D.C. current into any output	$\pm I_O$	max.	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100	mA
Total power dissipation	P_{tot}	max.	400	mW
Power dissipation per output	P_o	max.	100	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current					
through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at $V_{OH} = V_{SS}$ (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH					
during acknowledge (see Fig. 16)					
at $V_{OH} = V_{SS}$	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant$ 100 pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS peripheral circuit that functions as a real time clock/calendar with an Inter IC (I^2C) bus interface.
The device incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA are also available. Information is transferred via a serial, two-line bidirectional bus (I^2C). Back-up for the clock during supply interruption is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	–	6,0	V
Supply voltage (I^2C interface)		$V_{DD}-V_{SS2}$	2,5	–	6,0	V
Crystal oscillator		f_{osc}	–	32,768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

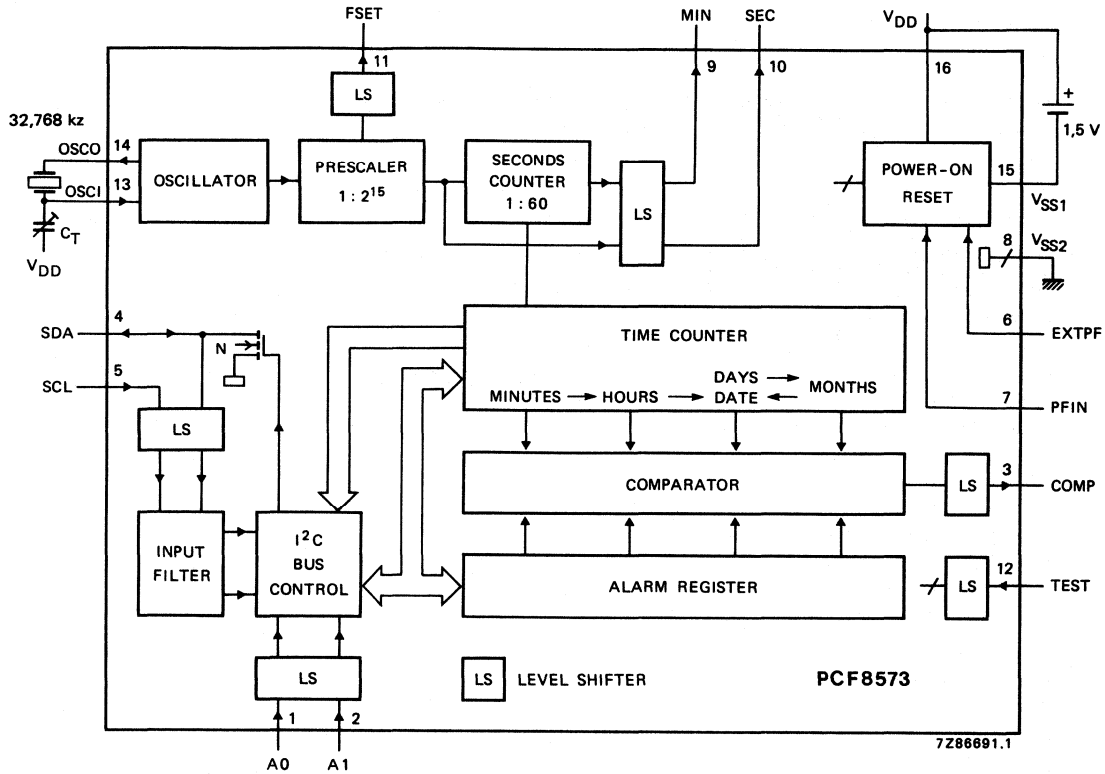


Fig. 1 Block diagram.

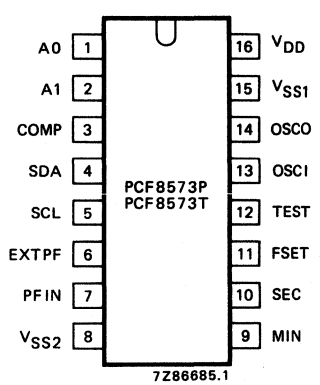


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

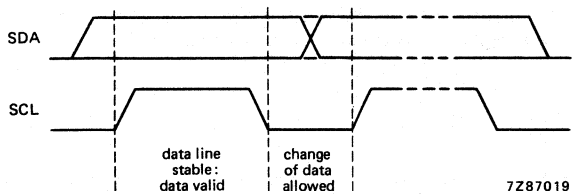


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

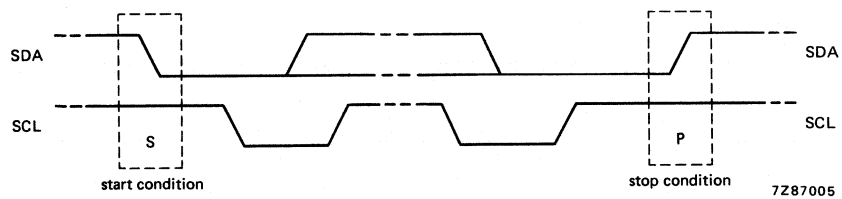


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

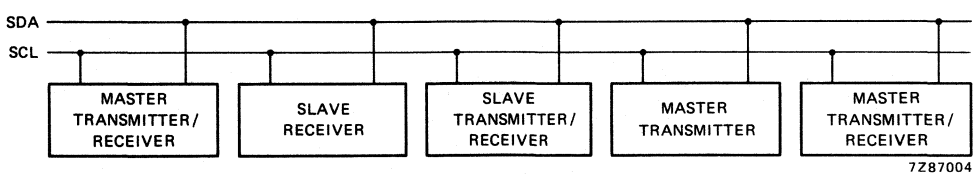


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 11 and Fig. 12.)

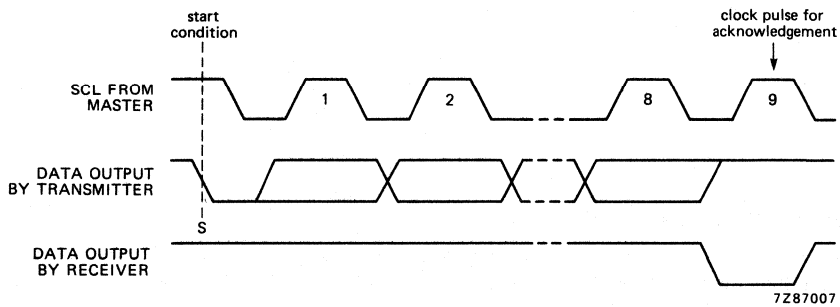


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

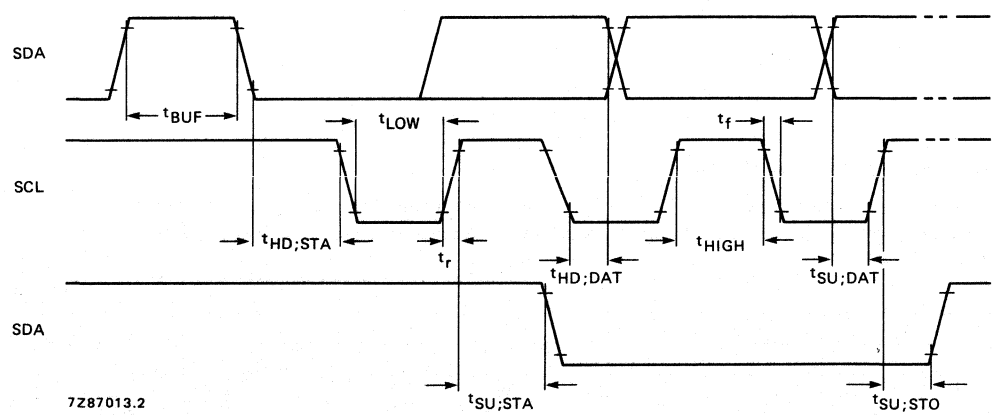


Fig. 7 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

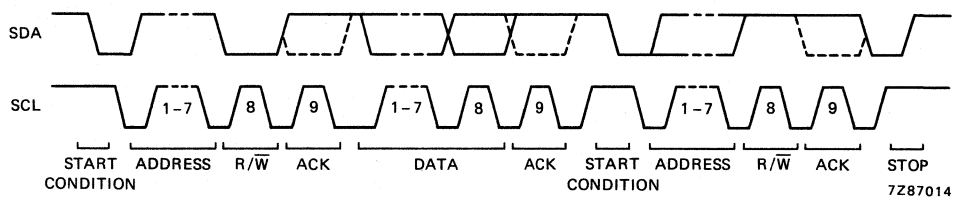


Fig. 8 Complete data transfer.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 9.

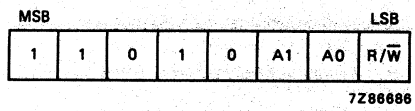


Fig. 9 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 10 and Fig. 11.

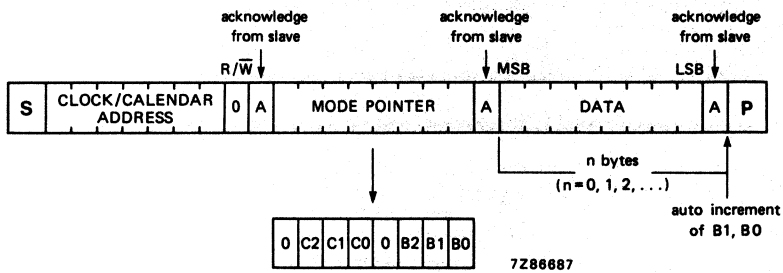


Fig. 10 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

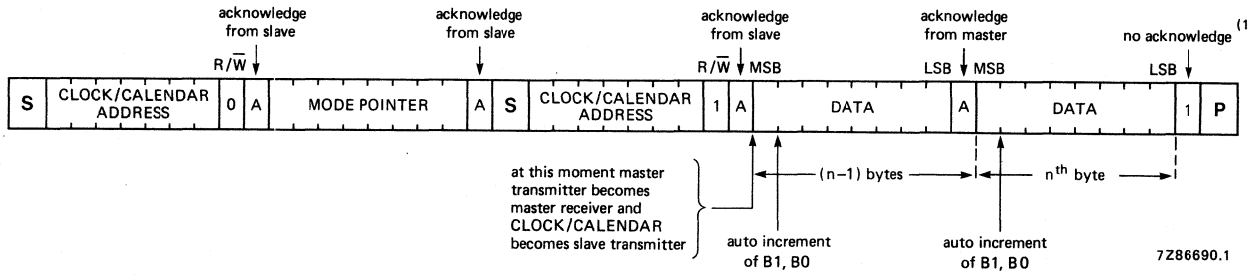
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

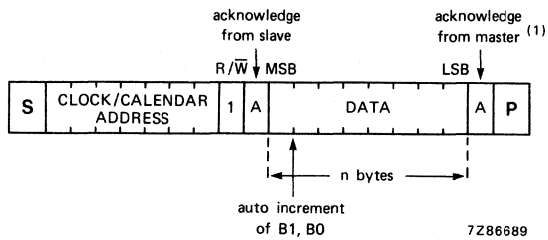
"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 11 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 12 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit.
* = minutes.
** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage ranges		$V_{DD}-V_{SS1}$	−0,3	8	V
		$V_{DD}-V_{SS2}$	−0,3	8	V
Voltage input (pins 4; 5)		V_I	$V_{SS2}-0,8$	$V_{DD}+0,8$	V*
Voltage input (pins 6; 7; 13, 14)		V_I	$V_{SS1}-0,6$	$V_{DD}+0,6$	V
Voltage on any other pin		V_I	$V_{SS2}-0,6$	$V_{DD}+0,6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage I^2C interface		$V_{DD}-V_{SS2}$	2,5	5,0	6,0	V
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	1,5	$V_{DD}-V_{SS2}$	V
Supply current V_{SS1}	$V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}	$V_{DD}-V_{SS2}$ = 5 V; (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current	$V_I = V_{SS2}$ to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN						
Input voltage HIGH		$V_{IH}-V_{SS1}$	0,7 x $V_{DD}-V_{SS1}$	–	–	V
Input voltage LOW		$V_{IL}-V_{SS1}$	0	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	1,0	μA
	T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	0,1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1,2	1,4	V
Power "ON" reset	$V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0,3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency at SCL	$V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (Fig. 7)		t_{LOW}	4,7	–	–	μs
Pulse width HIGH (Fig. 7)		t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input		T_I	0,25	1	2,5	μs
Input capacitance (SDA; SCL)		C_I	–	–	7	pF
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters	f = 32,768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	9	–	pF
Trimmer capacitance		C_T	5	–	25	pF

APPLICATION INFORMATION

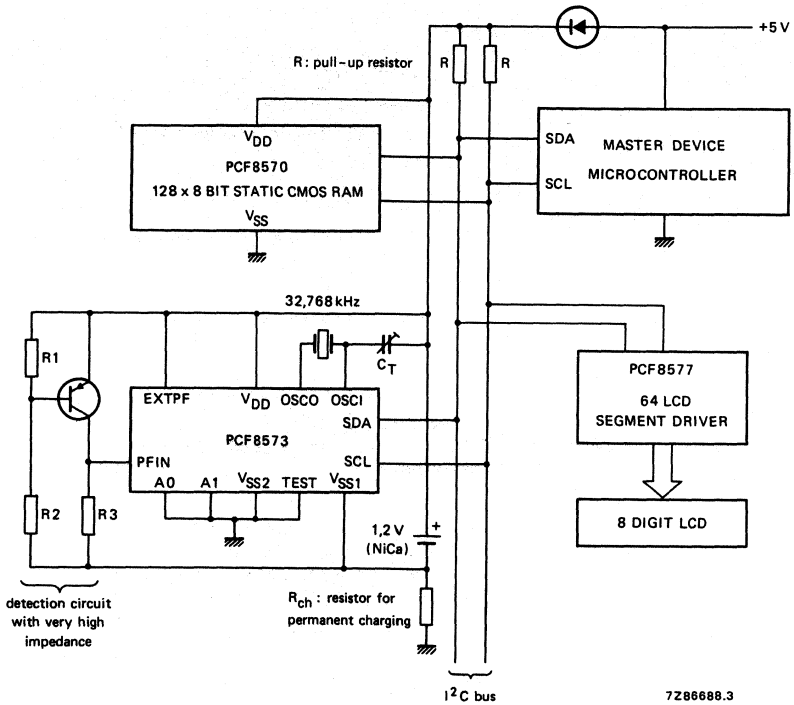


Fig. 13 Application example of the PCF8573 clock/calendar.

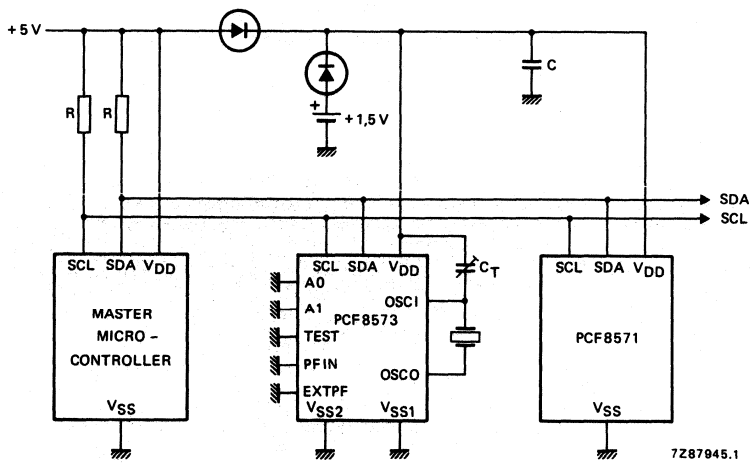


Fig. 14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

CLOCK CALENDAR WITH 256 × 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

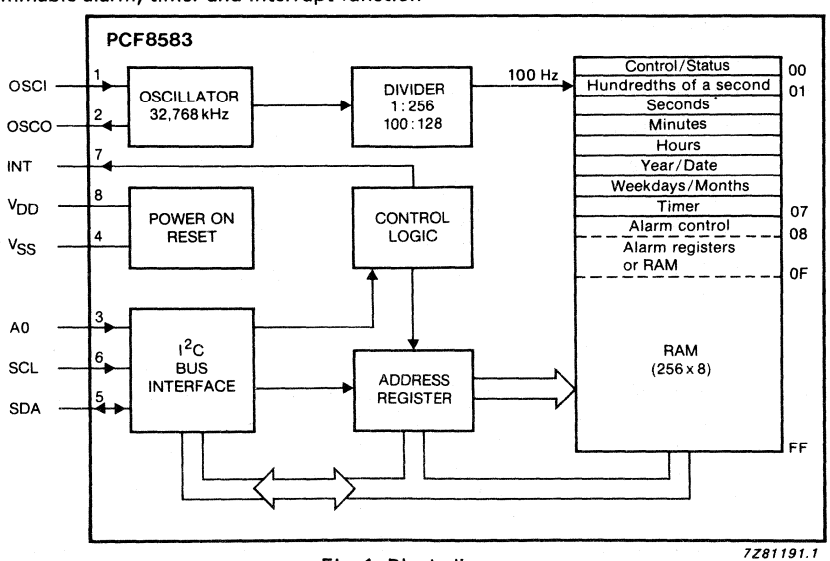


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT-97).
PCF8583T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input
2	OSCO	oscillator output
3	A0	address input
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	INT	open drain interrupt output (active low)
8	V_{DD}	positive supply

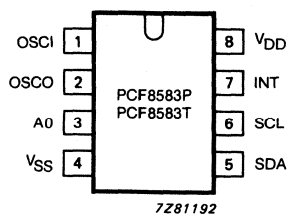


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V_{DD}	−0,8 to 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
DC input current (any input)	I_I	max. 10	mA
DC output current (any output)	I_O	max. 10	mA
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

Note

1. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

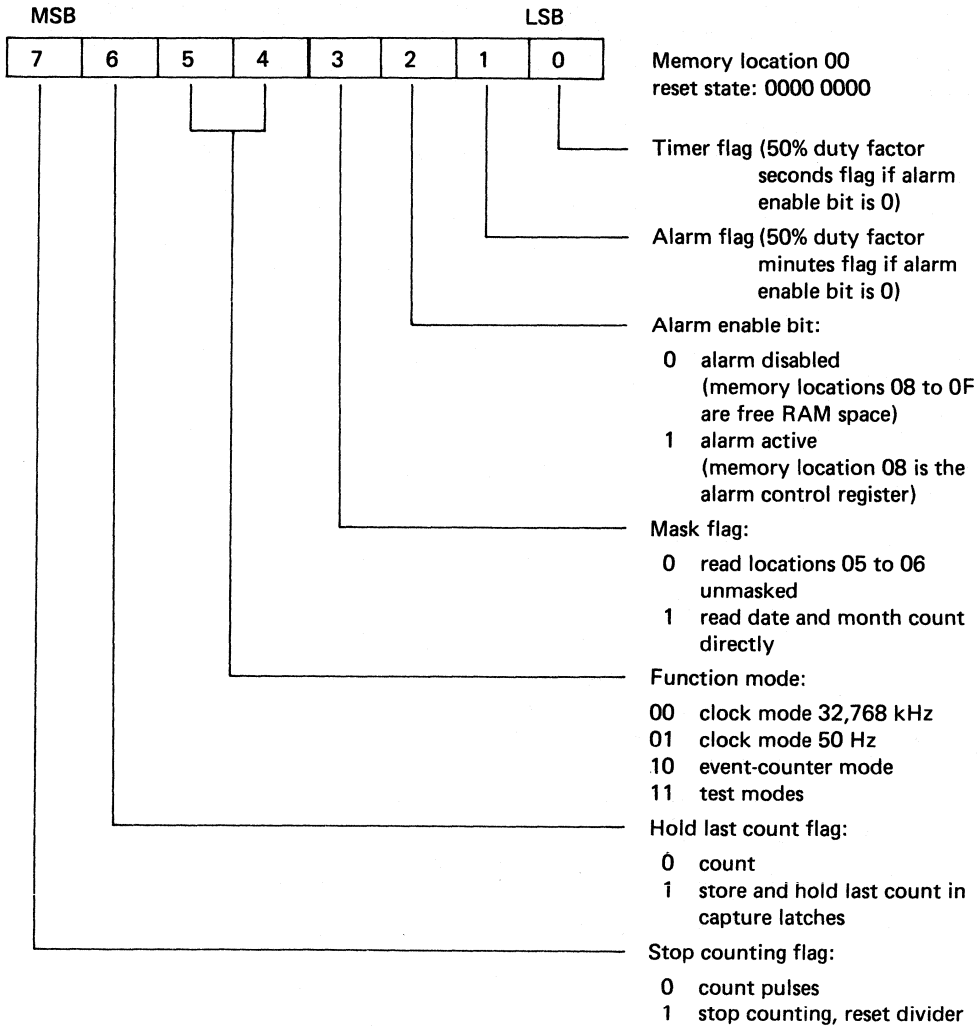


Fig. 3 Control/status register.

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

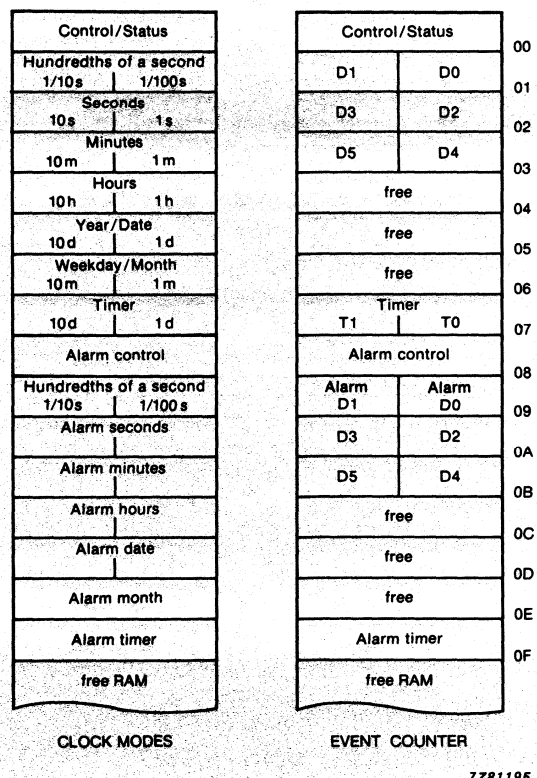


Fig. 4 Register arrangement.

Counter registers (continued)

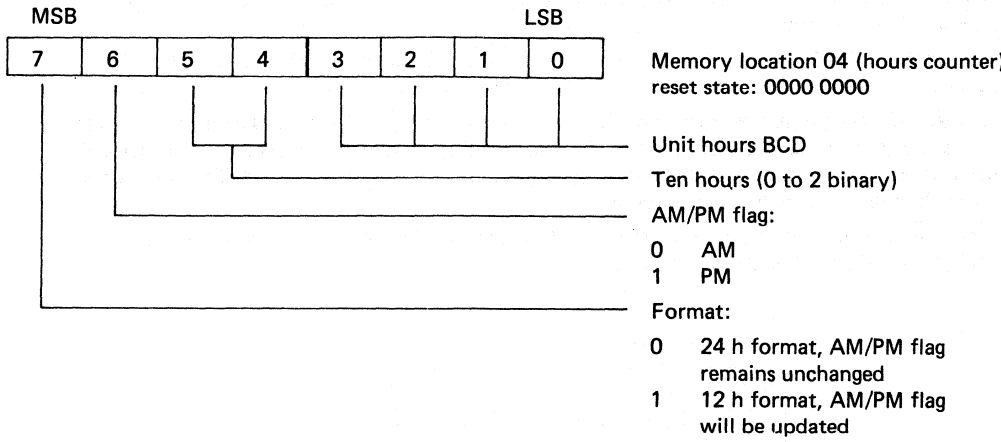


Fig. 5 Format of the hours counter.

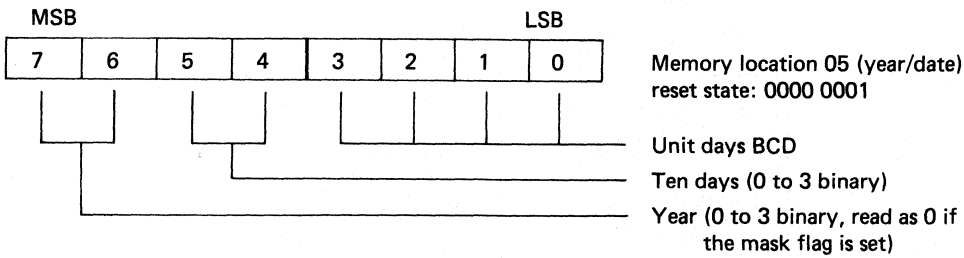


Fig. 6 Format of the year/date counter.

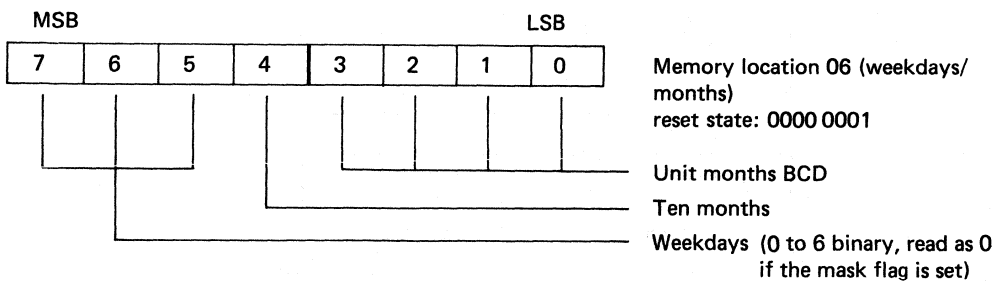


Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

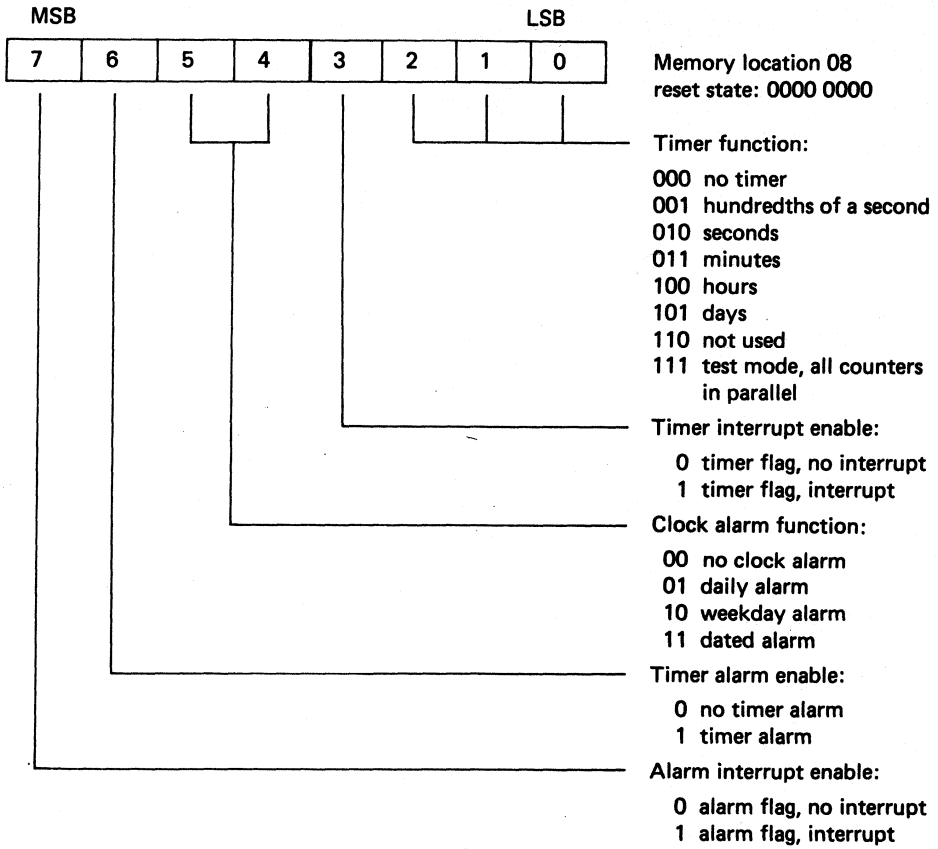


Fig. 8a Alarm control register, clock modes.

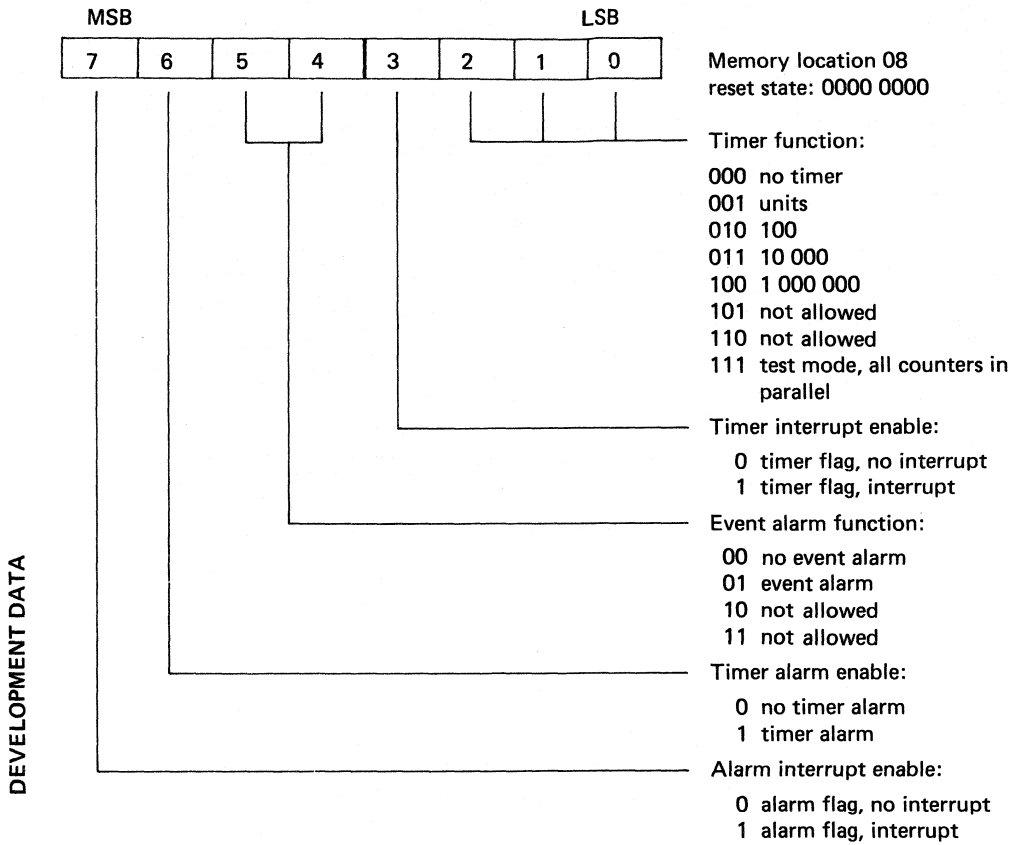


Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

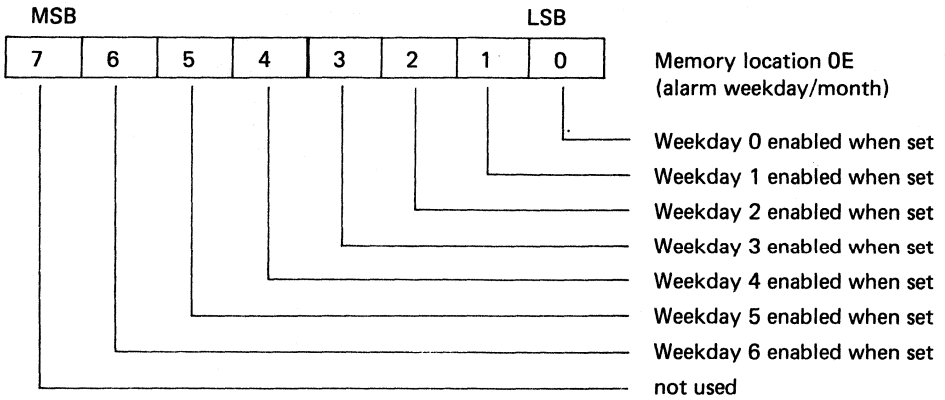


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I^2C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

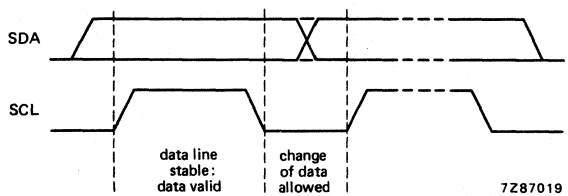


Fig. 10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

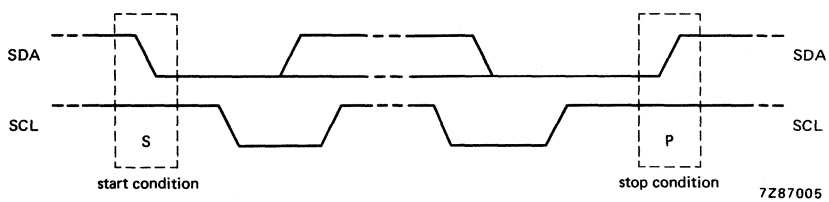


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

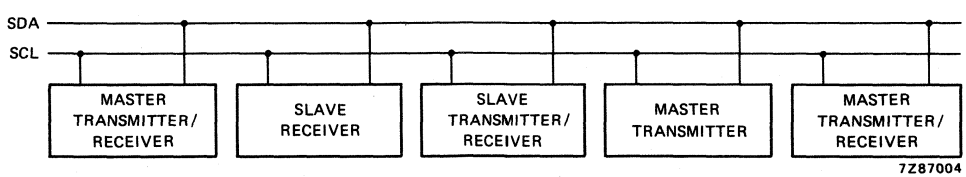


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

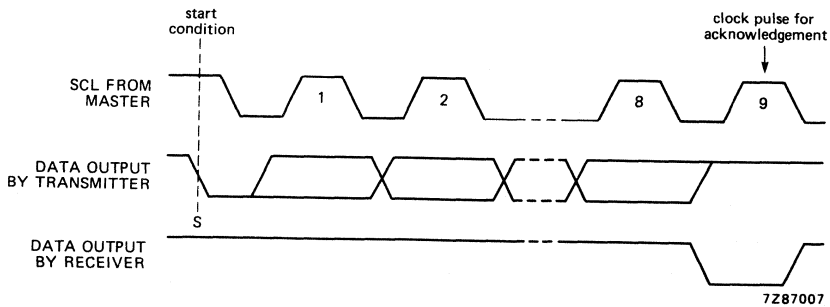


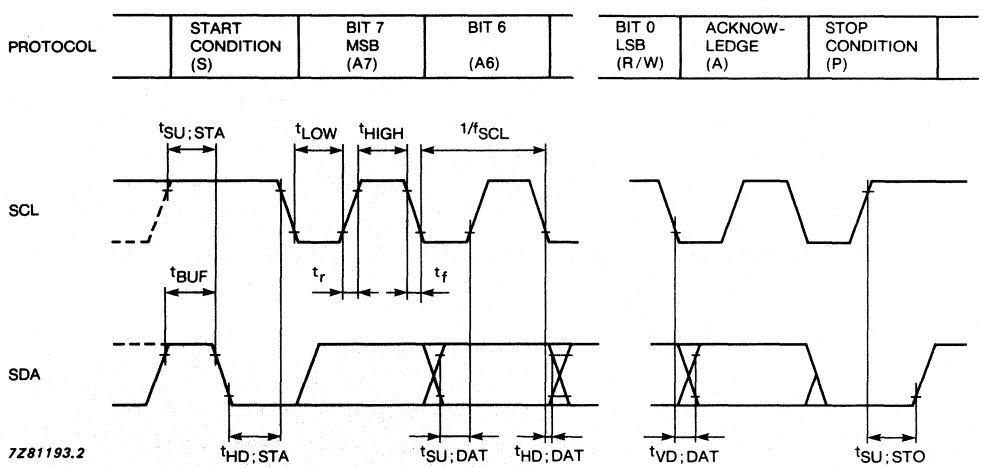
Fig. 13 Acknowledgement on the I²C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs



I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

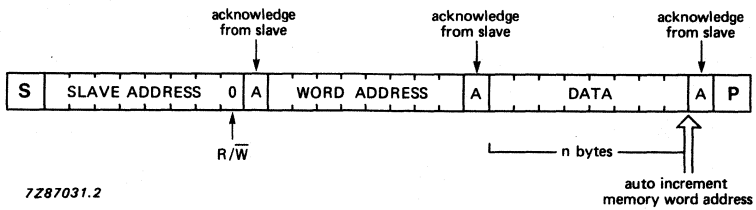


Fig. 15a Master transmits to slave receiver (WRITE mode).

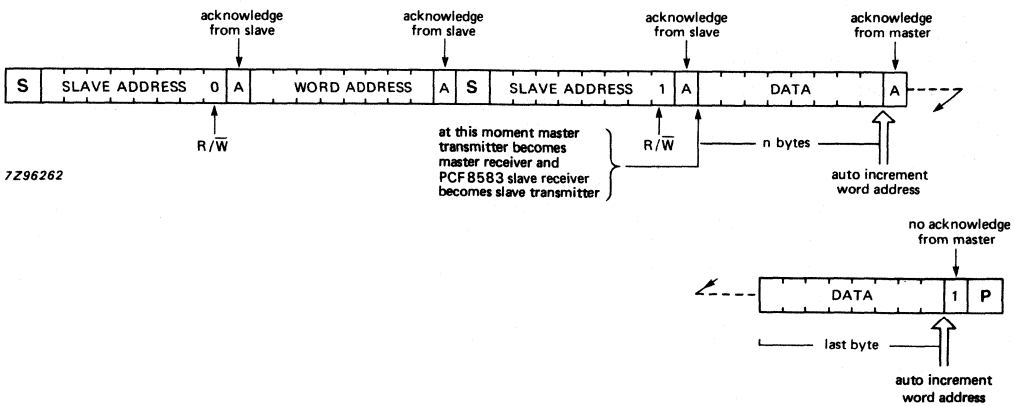


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

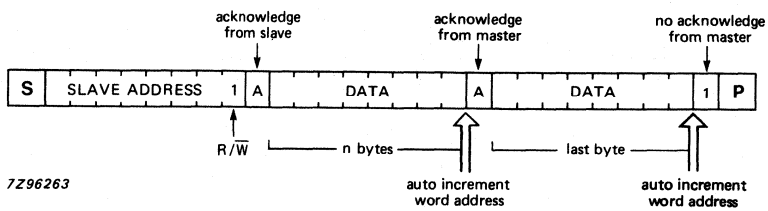


Fig. 15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2,0 to 6,0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (operating)	V_{DD}	2,5	–	6	V
Supply voltage (clock)	V_{DD}	1,0	–	6	V
Supply current					
T_{amb} = 0 to 70 °C operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
Clock at V_{DD} = 5 V	I_{DDO}	–	10	50	μA
Clock at V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW (note 2)	V_{IL}	–0,8	–	0,3 x V_{DD}	V
Input voltage HIGH (note 2)	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
Input leakage current at V_I = V_{DD} or V_{SS}	± I_I	–	–	250	nA
Input capacitance (SCL, SDA) at V_I = V_{SS}	C_I	–	–	7	pF
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V (note 3)	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = –25 to + 70 °C (note 3)	I_{DDR}	–	–	2	μA
Oscillator					
Integrated oscillator capacitance	C_{OSC}	–	40	–	pF
Oscillator stability for: ΔV_{DD} = 100 mV at V_{DD} = 1,5 V; T_{amb} = 25 °C	f/f_{OSC}	–	2×10^{-6}	–	–

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	KΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.
3. Event or 50 Hz mode only (no Quartz).

DEVELOPMENT DATA

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

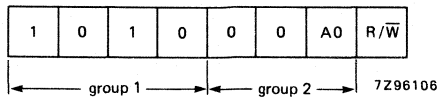


Fig. 16 PCF8583 address.

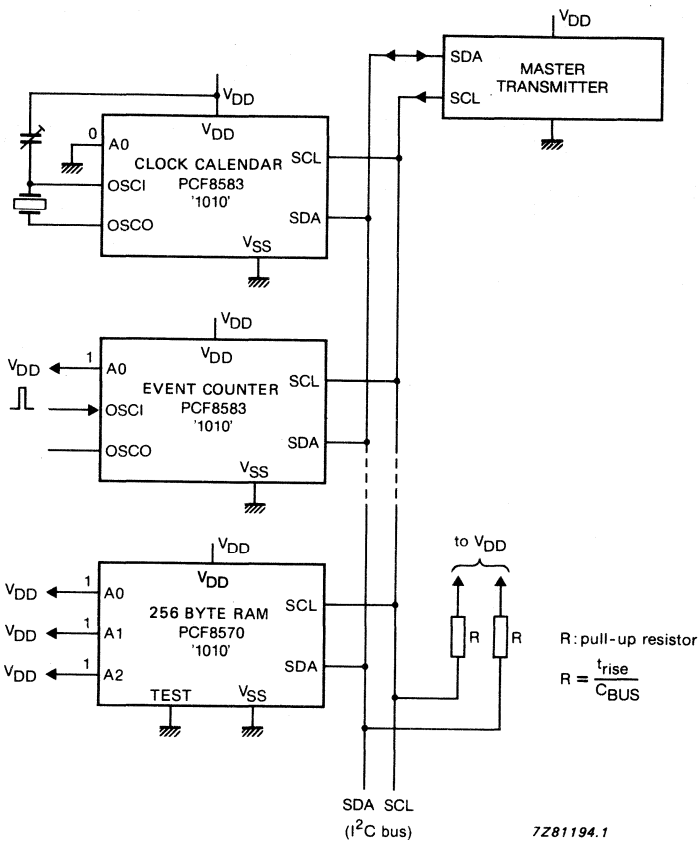


Fig. 17 PCF8583 application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

128 x 8 BIT/256 x 8 BIT STATIC RAMs WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

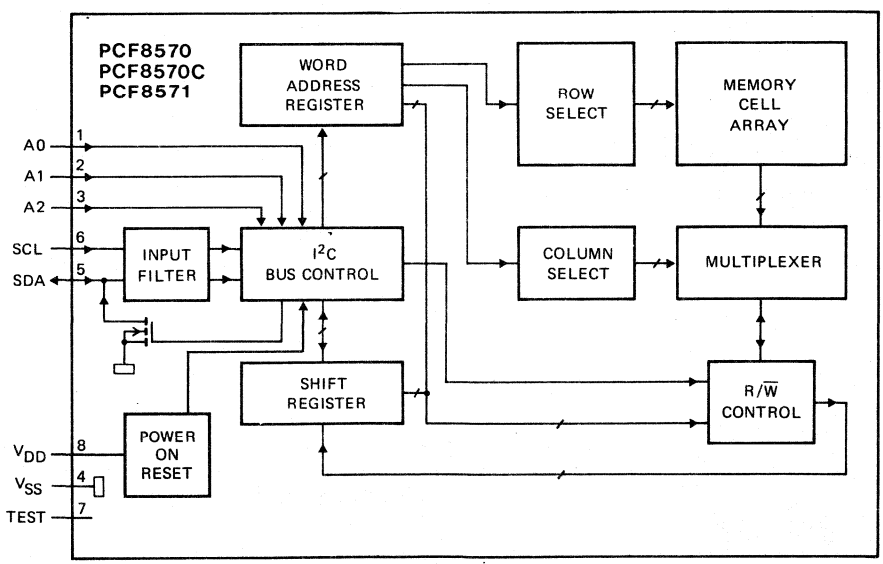


Fig. 1 Block diagram. 7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT-97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO-8L; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C bus)
6	SCL	serial clock line (I²C bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

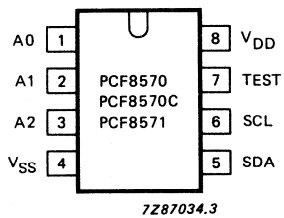


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}	−0,8 to + 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
DC input current (any input)	$\pm I_I$	max. 10	mA
DC output current (any output)	$\pm I_O$	max. 10	mA
Supply current (pin 8 or pin 4)	$\pm I_{DD}$; I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD};					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 12 and 13)					
Supply current at T_{amb} = 25 °C; TEST = V_{DD};					
PCF8570/8570C	I_{DDR}	–	50	400	nA
PCF8571	I_{DDR}	–	50	200	nA
Recovery time	t_{HD2}	–	50	–	μs

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

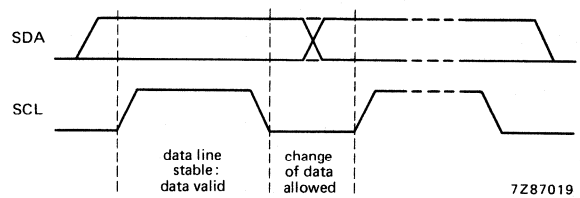


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

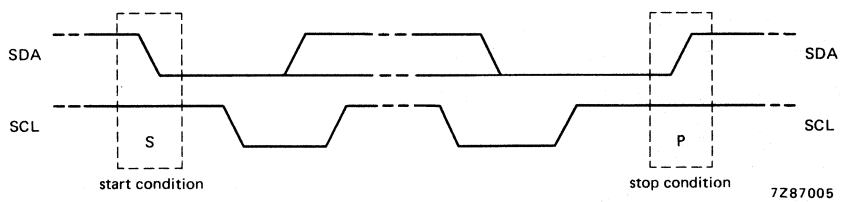


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

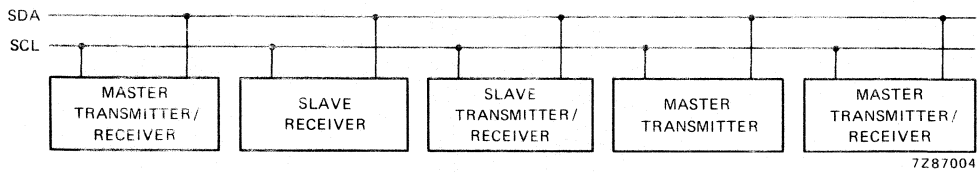


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

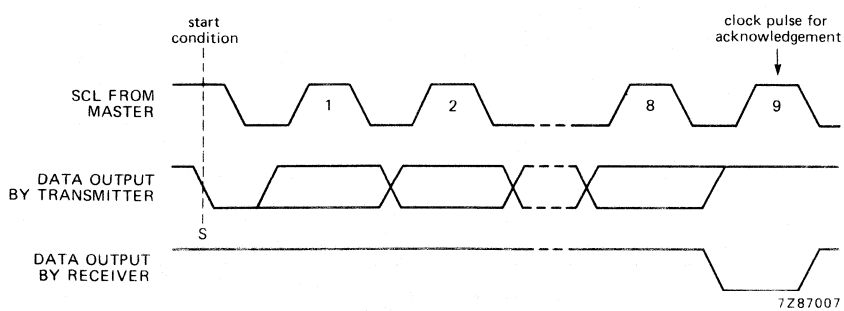


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

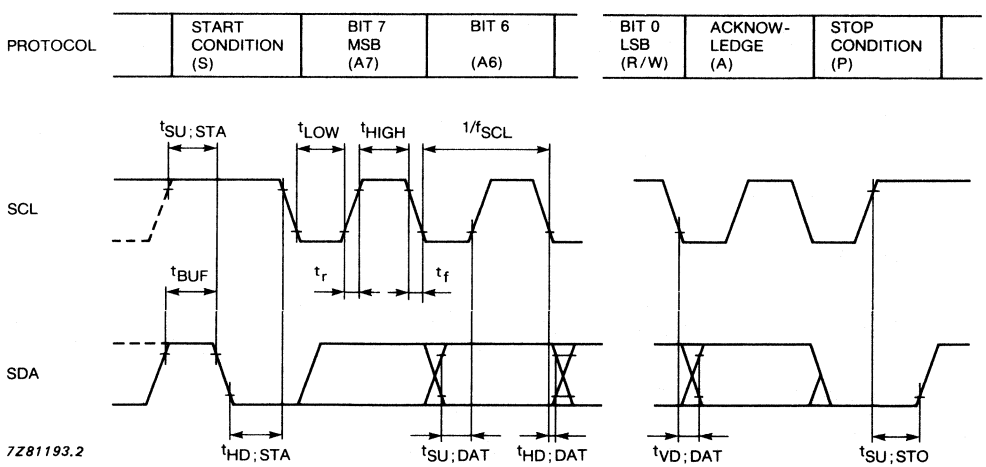


Fig. 7 I²C bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig. 8.

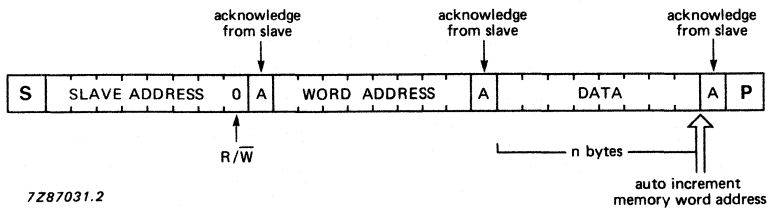


Fig. 8(a) Master transmits to slave receiver (WRITE mode).

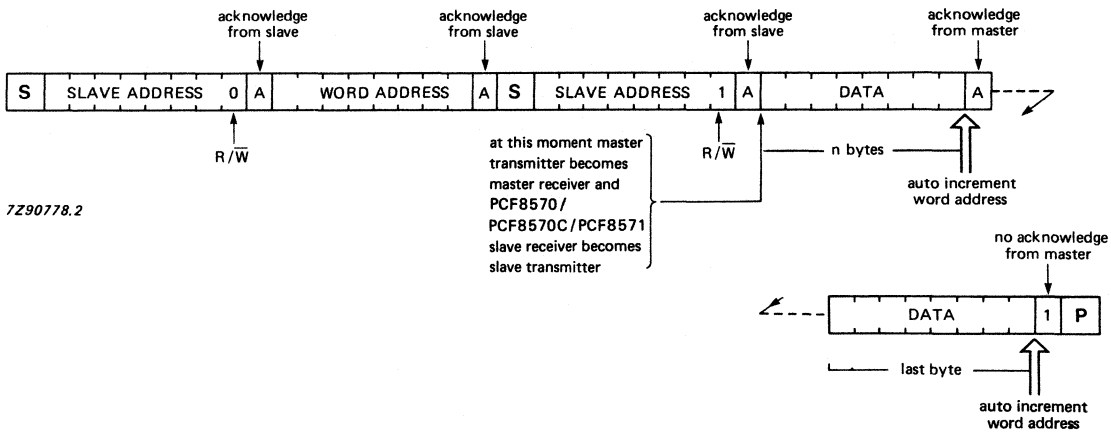


Fig. 8(b) Master reads after setting word address (WRITE word address; READ data).

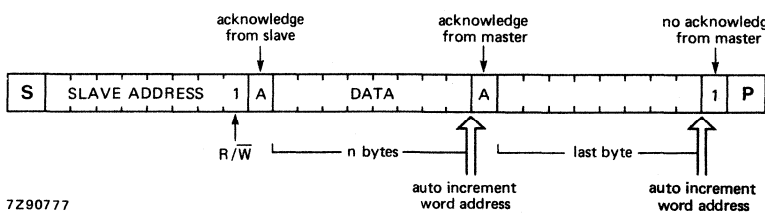


Fig. 8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig. 10).

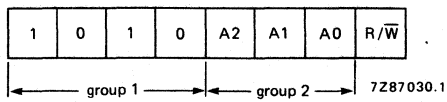


Fig. 9 PCF8570 and PCF8571 address.

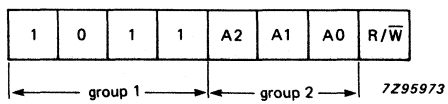


Fig. 10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

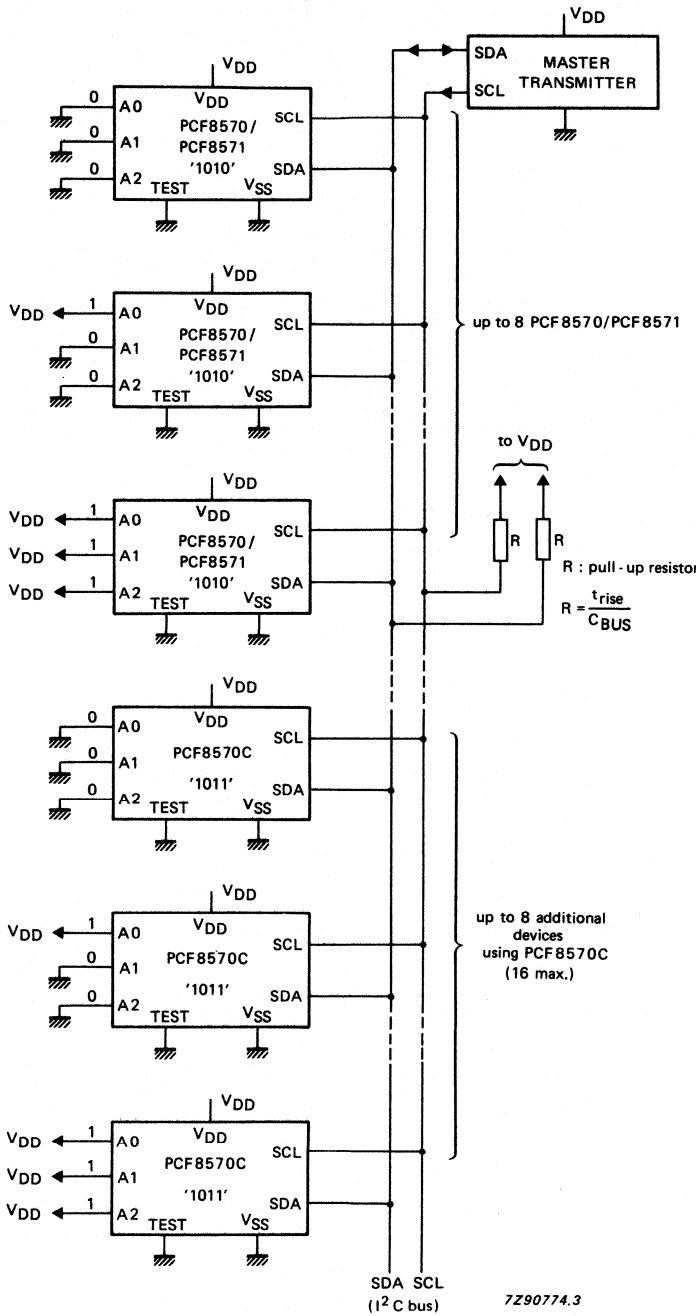
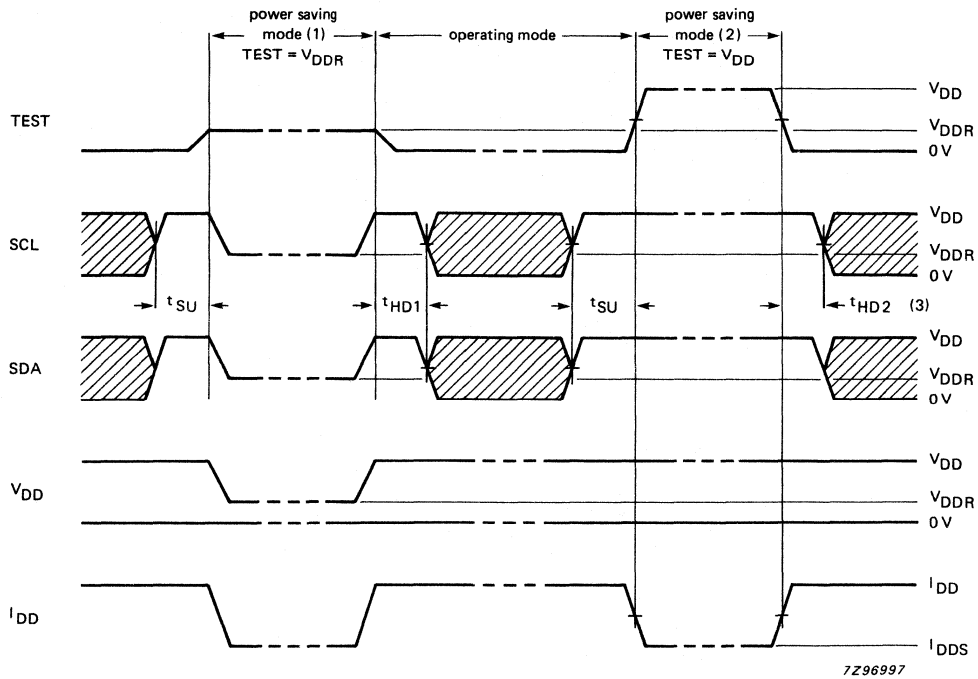


Fig. 11 Application diagram.

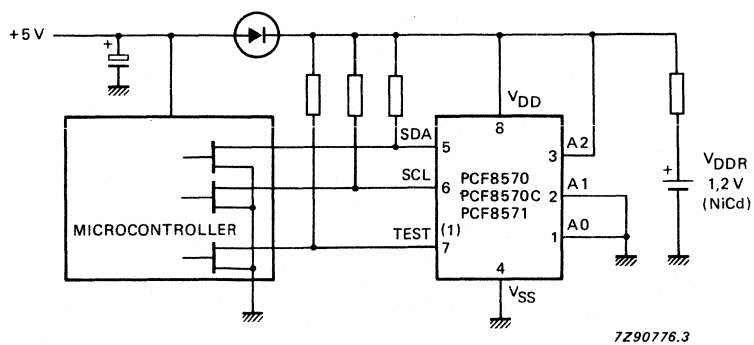
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig. 12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

Fig. 13 Application example for power saving mode.

256 × 8-bit STATIC CMOS EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator. If the latter is used an RC time constant must be connected to pin 7 or 13.

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

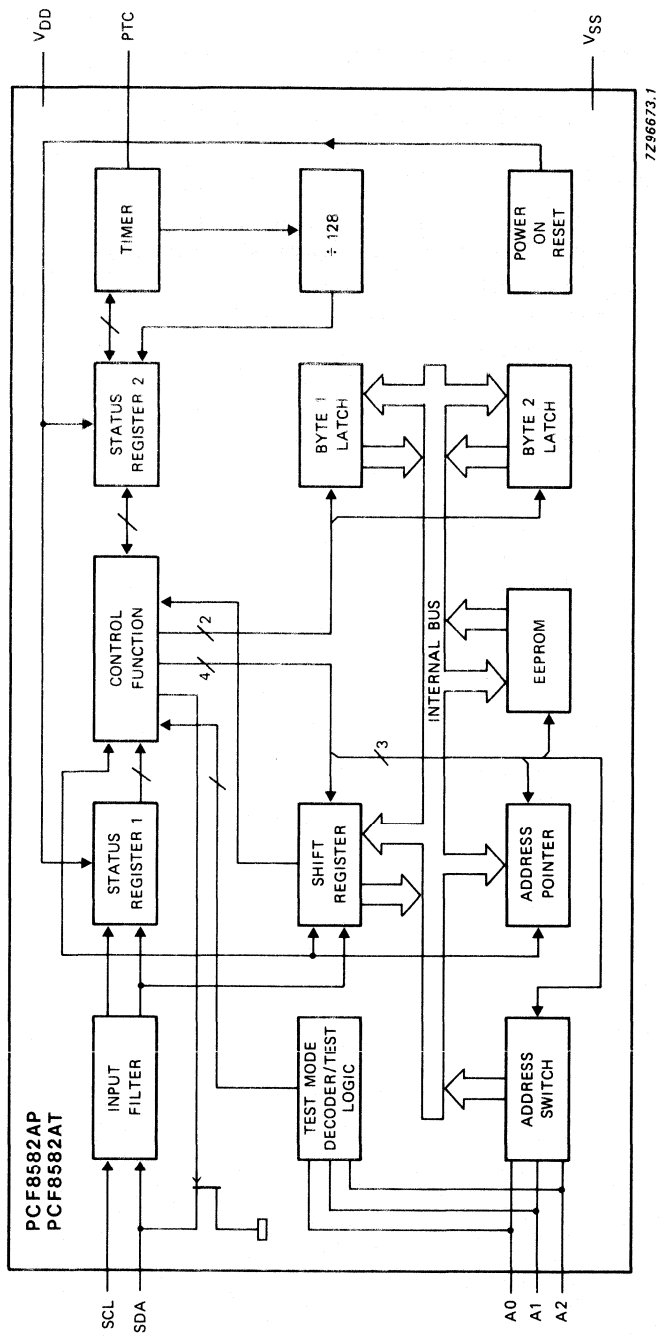
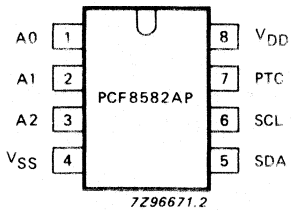
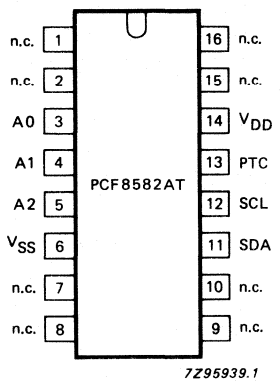


Fig. 1 Block diagram.



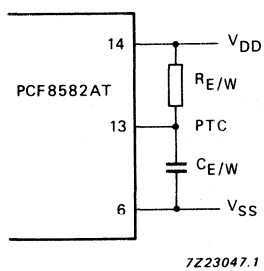
1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I²C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

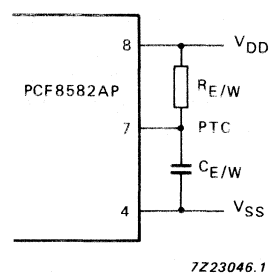
Fig. 2 (a) Pinning diagram.



1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I²C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.





Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

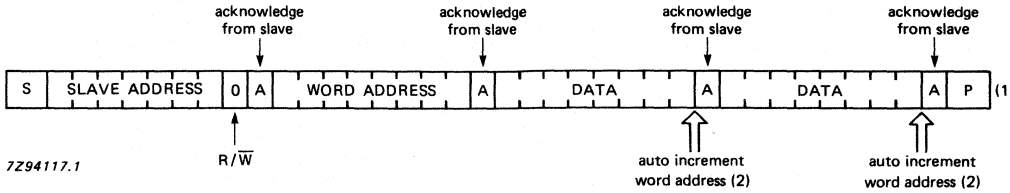
Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I²C-bus are available on request.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

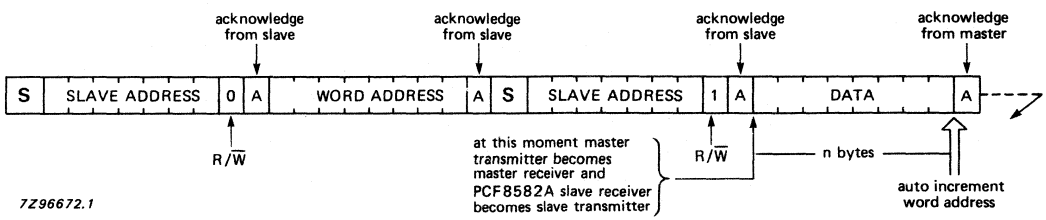
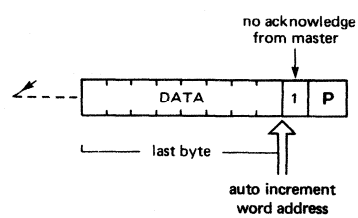


Fig. 4(b) Master reads PCF 8582A slave after setting word address (write word address; READ data).



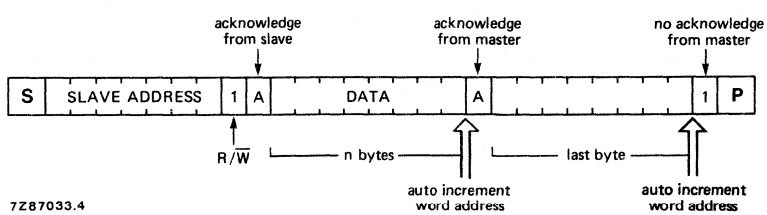


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

* The device can be used as read only without the programming clock.

I²C-bus timing

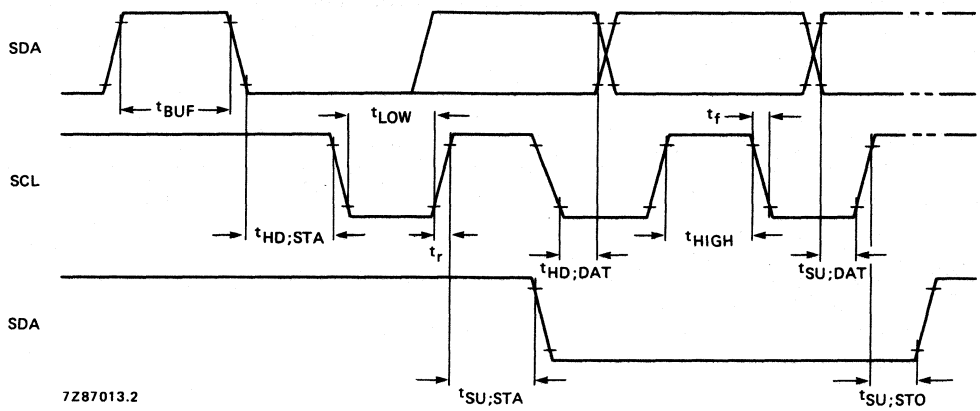
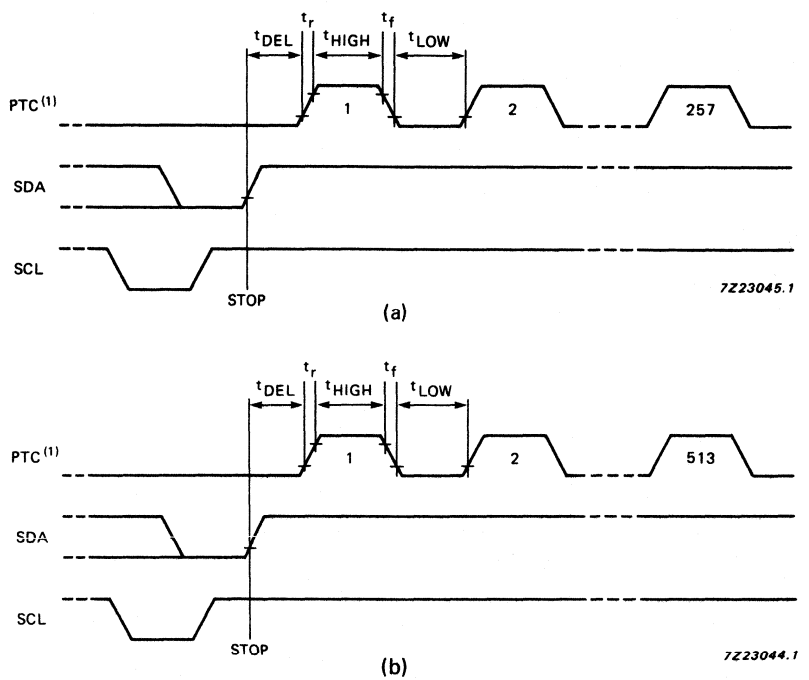


Fig. 5 I²C-bus timing.



(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	–	1	mA
Output current	$\|I_O\|$	–	10	mA

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	V_{OH} = V_{DD}	I_{LO}	–	–	1	μA
Input leakage current (SCL)	V_I = V_{DD} or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1.	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	20	–	100	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	2.57	–	12.85	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P: 16-lead DIL; plastic (SOT-38).
PCF8591T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

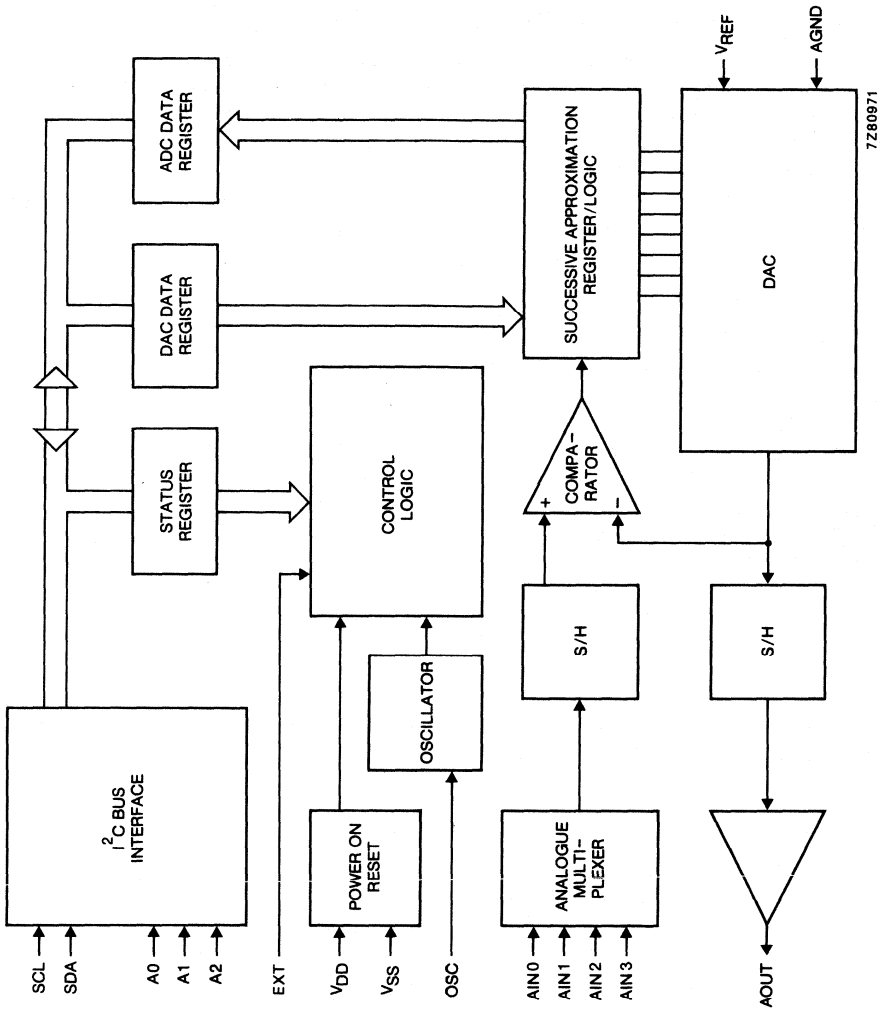


Fig. 1 Block diagram.

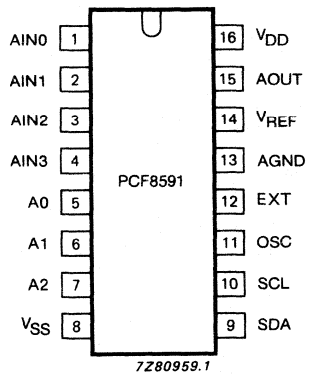


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

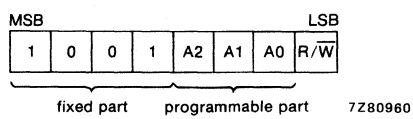


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

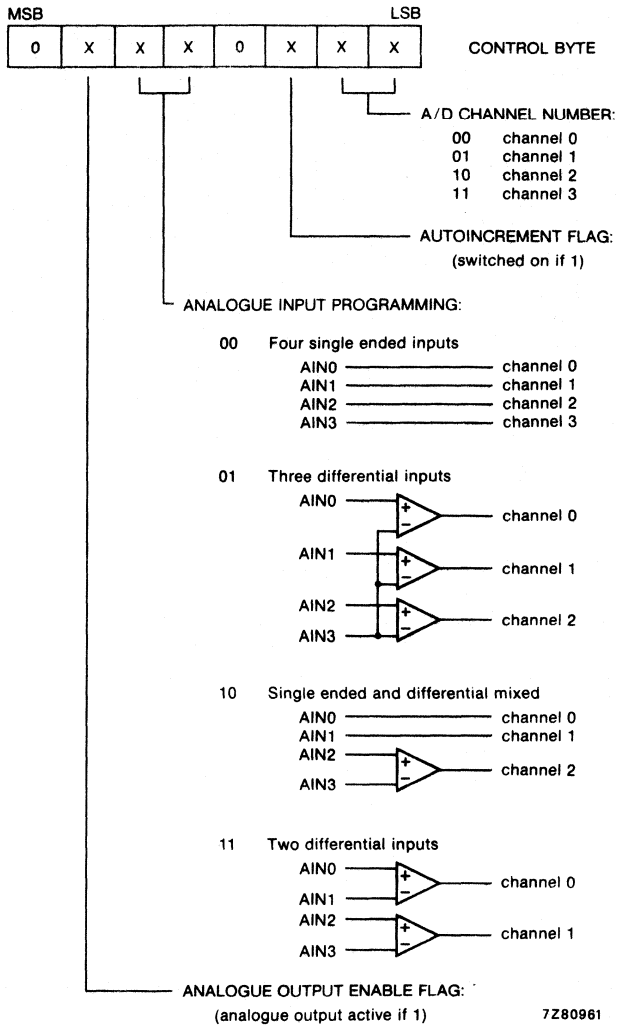


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

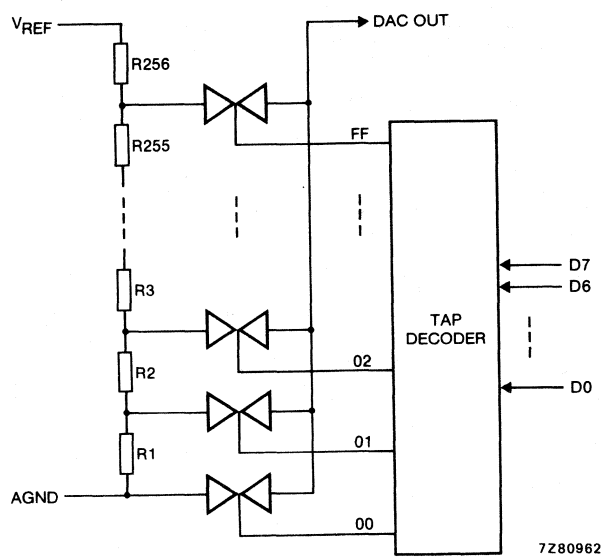


Fig. 5 DAC resistor divider chain.

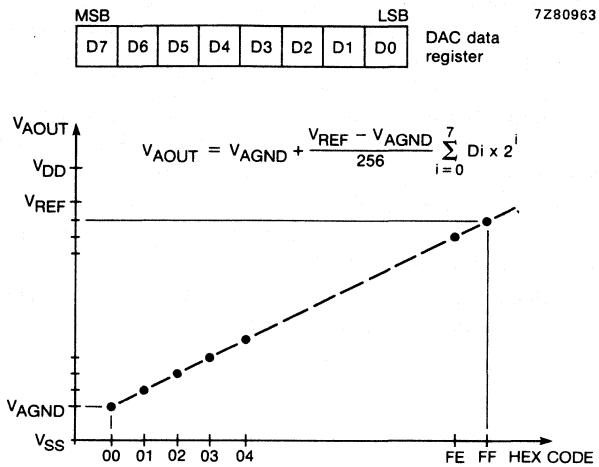


Fig. 6 DAC data and d.c. conversion characteristics.

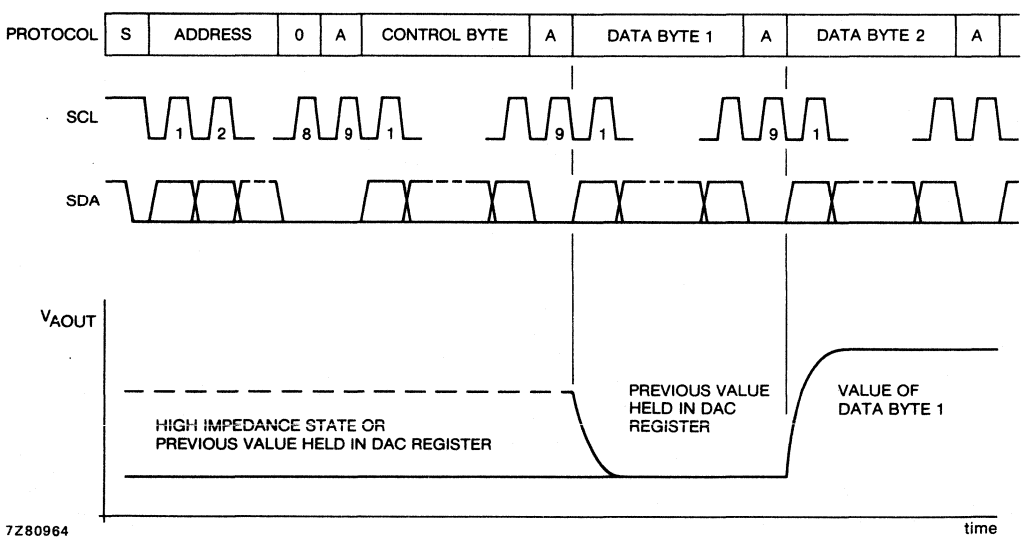


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

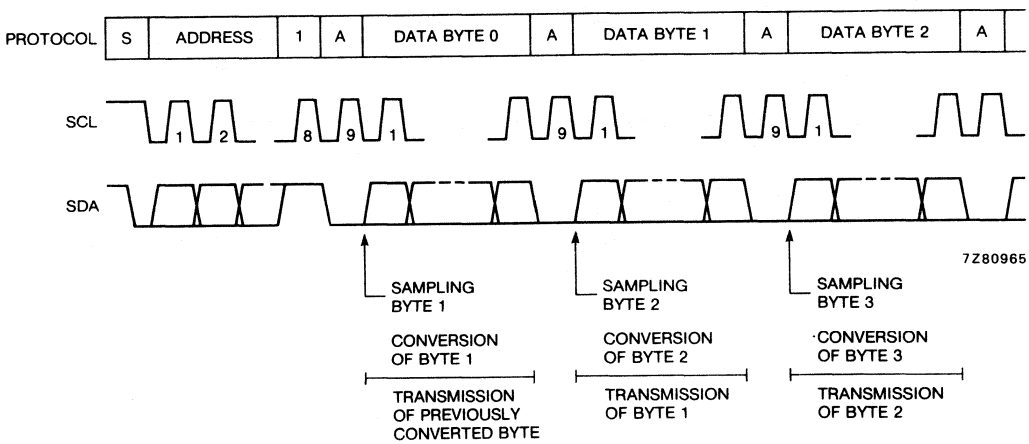


Fig. 8 A/D conversion sequence.

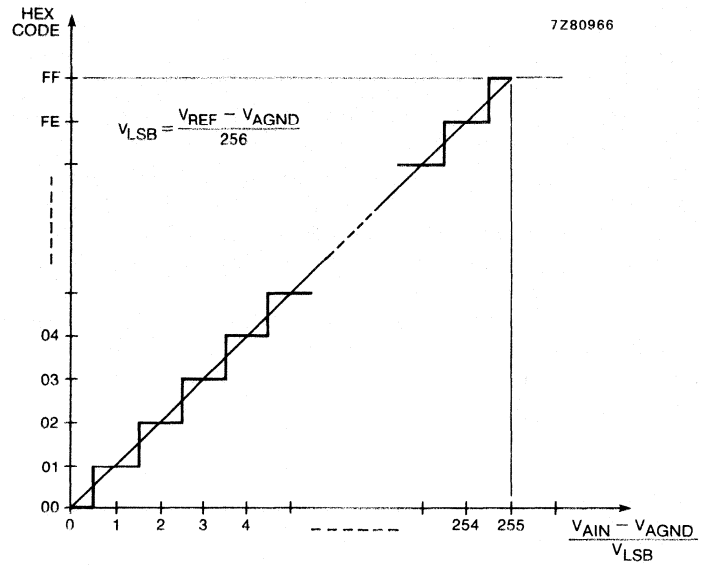


Fig. 9a A/D conversion characteristics of single-ended inputs.

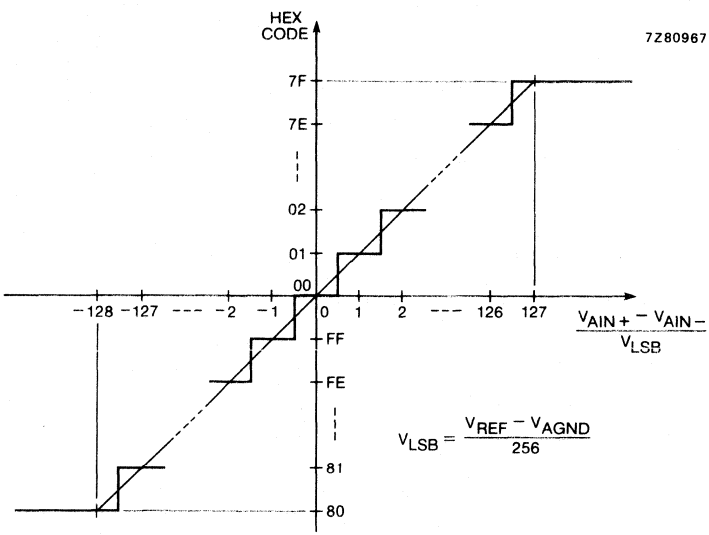


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

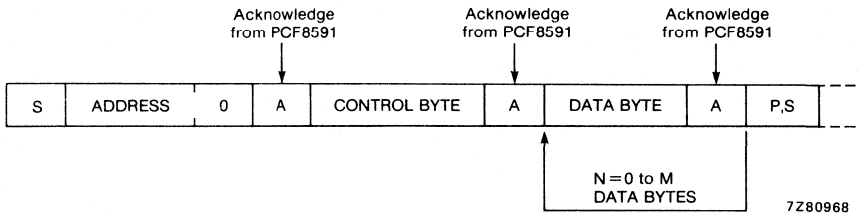


Fig. 10a Bus protocol for write mode, D/A conversion.

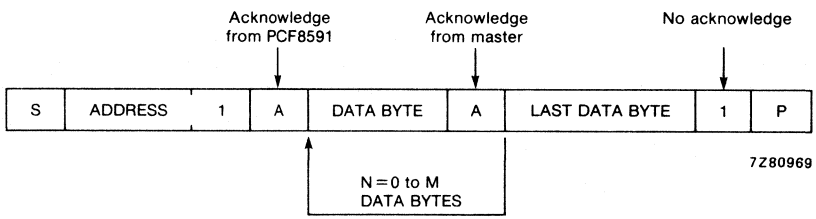


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

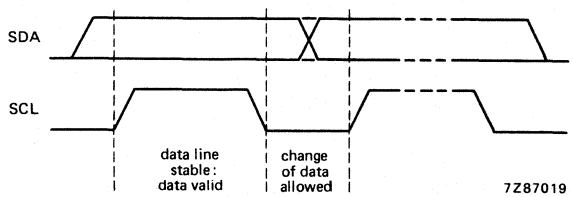


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

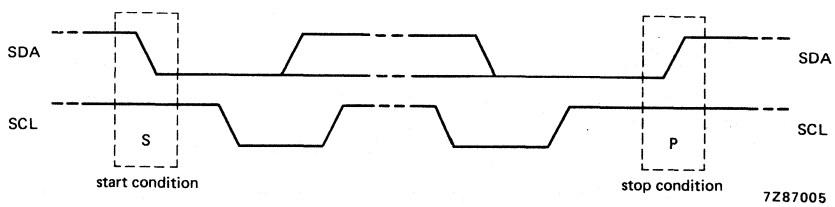


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

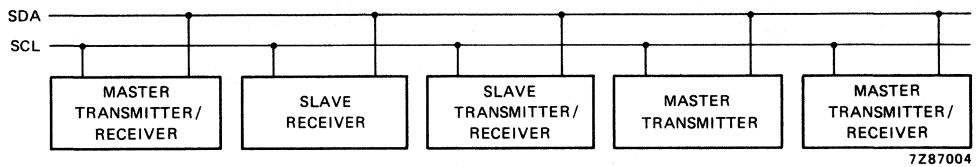


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

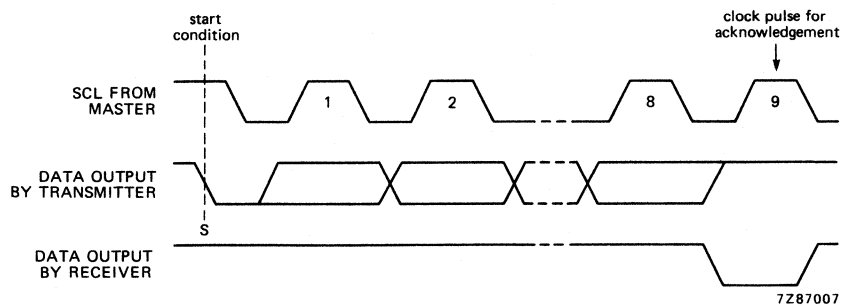


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

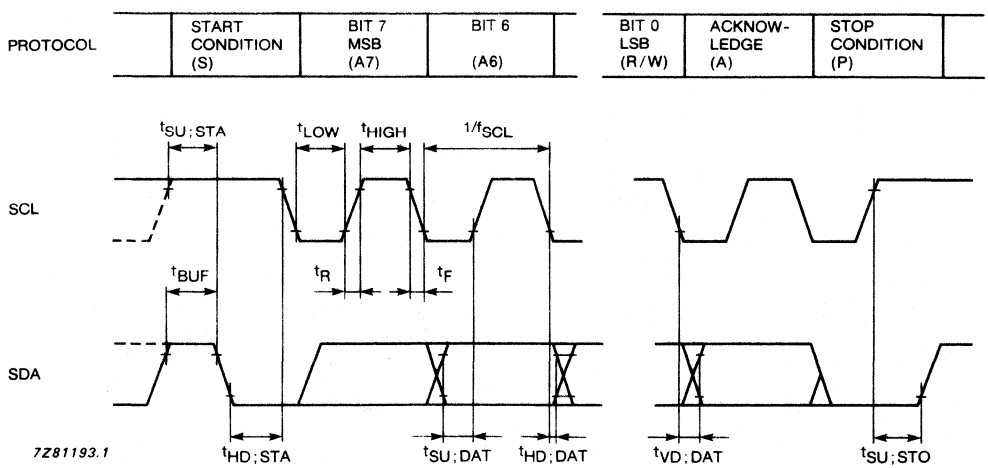


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby V_I = V_{SS} or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; V_I = V_{SS} to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

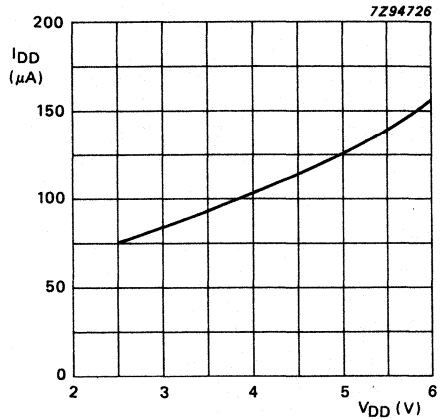
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

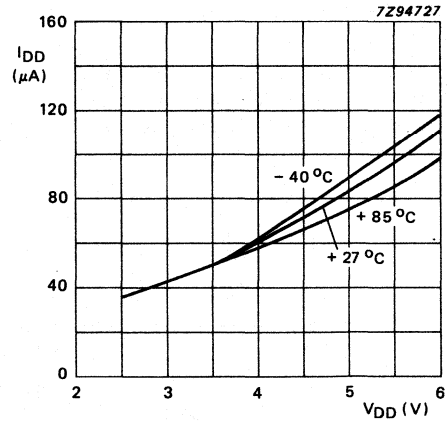
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



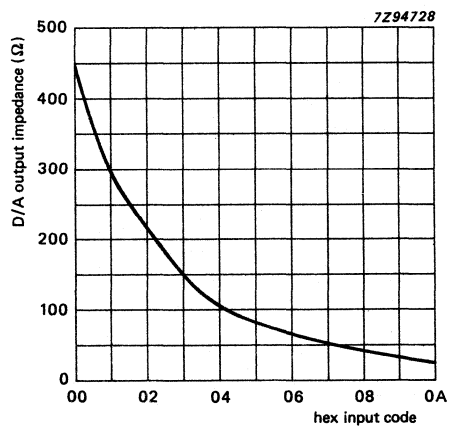
(a) internal oscillator; T_{amb} = + 27 °C.



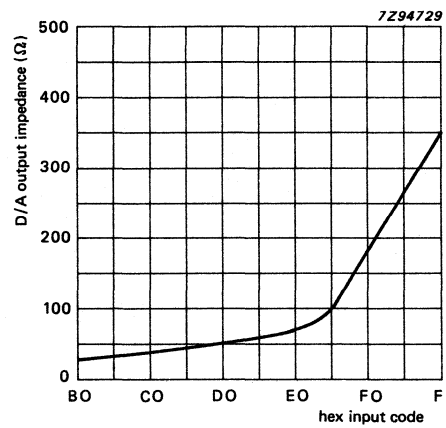
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

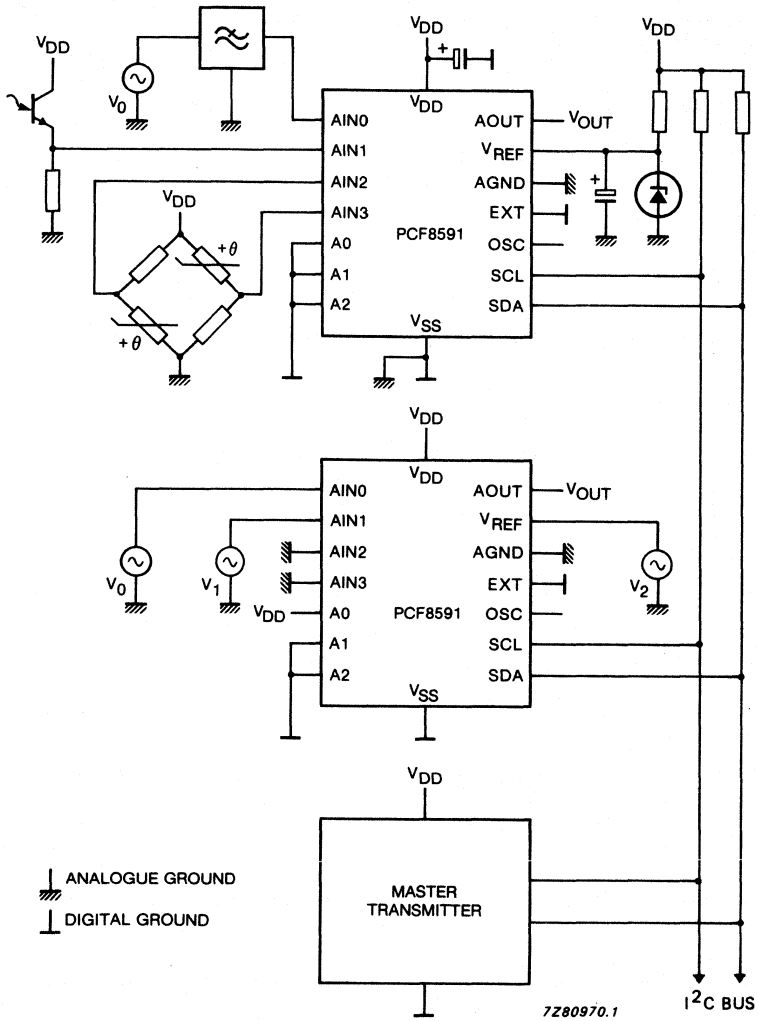


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

LCD DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,2 to 5,5	V
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Maximum input frequency	f_i	typ. 50	kHz
Supply current	I_{CC}	typ. 3,5	mA
Output current (Q_1 to Q_{20})	I_Q	> 60	μA

PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

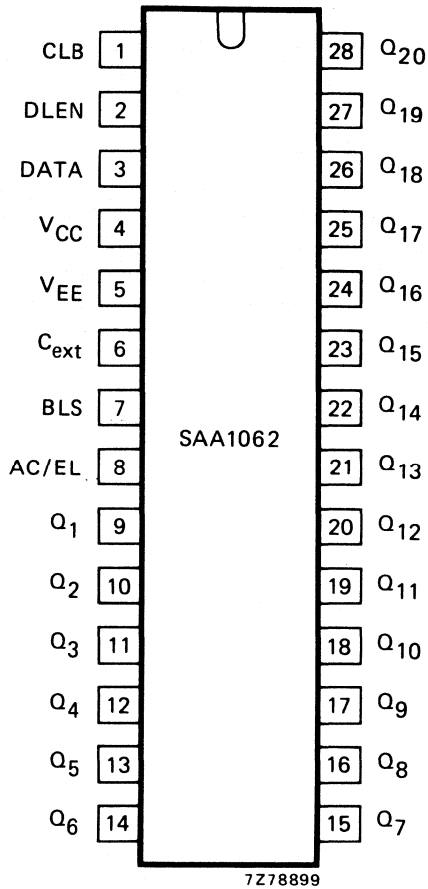


Fig. 1 Pinning diagram.

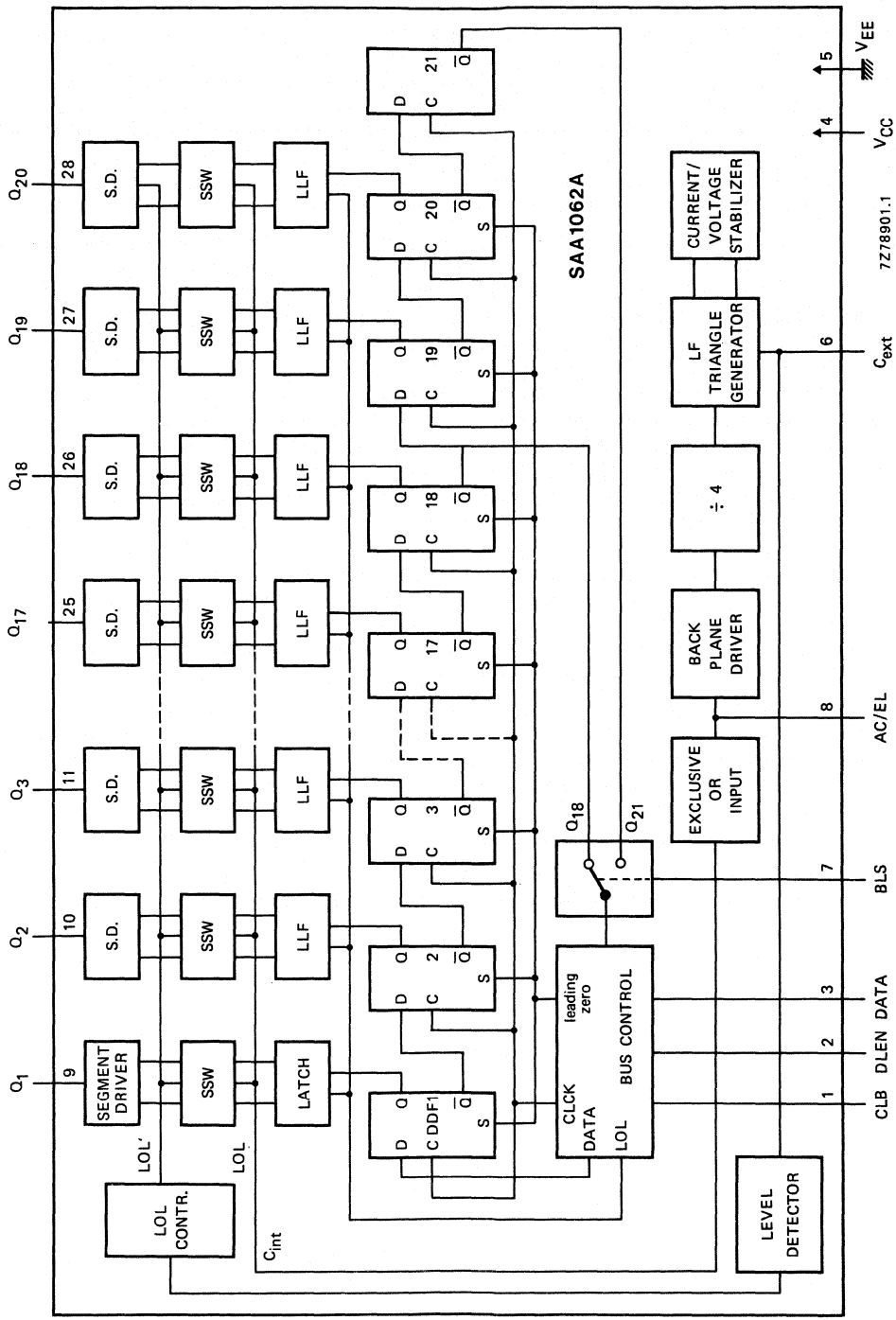


Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).

This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.

The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180^{o} out-of-phase when the input data is LOW ("0").

In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or V_{CC}. The IC now can operate as a static driver or as a synchronized slave.

The I.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

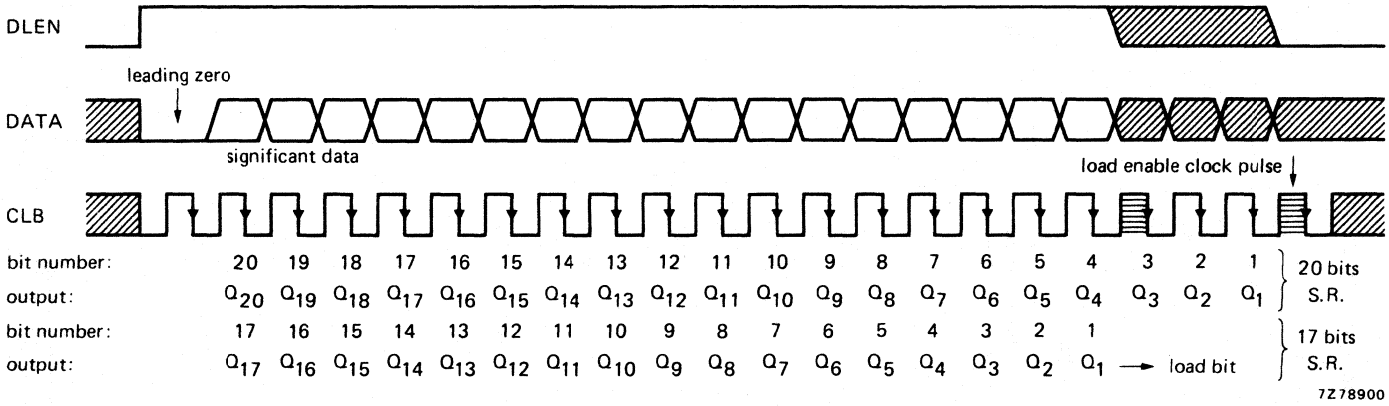


Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment 'on'.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6 V
Total power dissipation at T_{amb} = 100 °C derate linearly with 0,02 W/°C	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−25 to + 125 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		condition
Supply voltage	V_{CC}	4,2	5	5,5	V	
Supply current	I_{CC}	–	3,5	–	mA	
Inputs CLB, DLEN, DATA, BLS						
input voltage HIGH	V_{IH}	1,6	–	V_{CC}	V	
input voltage LOW	V_{IL}	−1	–	+ 0,8	V	
maximum input frequency	f_I	–	50	–	kHz	
Input C_{ext}						
input voltage HIGH	V_{IH}	4,6	–	–	V	static mode
input voltage LOW	V_{IL}	−0,1	–	0,4	V	sync. slave mode
input current HIGH	I_{IH}	–	–	180	μA	
input current LOW	I_{IL}	–	–	−40	μA	
Input AC/EL (in slave mode)						
input voltage HIGH	V_{IH}	2,7	–	V_{CC}	V	
input voltage LOW	V_{IL}	−0,4	–	2,3	V	
Output C_{ext} (oscillator mode)						
oscillator frequency	f_{osc}	120	240	360	Hz	C = 22 nF
Output stage backplane (AC/EL)						
output current sink/source	I_O	2,4	–	–	mA	
Output Q_1 to Q_{20}						
output current sink/source	I_O	60	–	–	μA	
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)						
segment 'on' situation		–	–	25	mV	
segment 'off' situation		–	–	25	mV	

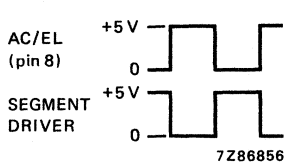


Fig. 4 AC/EL and segment driver pulses.
The d.c. voltage for segment 'on' is about 5 V.

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DATA HANDBOOK SYSTEM

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